DDR4 SDRAM Specification

CAUTION :
The 3DS contents in this document includes some items still under discussion in JEDEC
Therefore, those may be changed without pre-notice based on JEDEC progress
In addition, it is highly recommended that you not send specs without Samsung's permission

Device Operation & Timing Diagram

Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	- First Spec release	Sep. 2014	-	J.Y.Lee
1.1	- Add 3DS Functional Description,3DS SDRAM Command Description and Operation	Oct. 2014	-	J.Y.Lee

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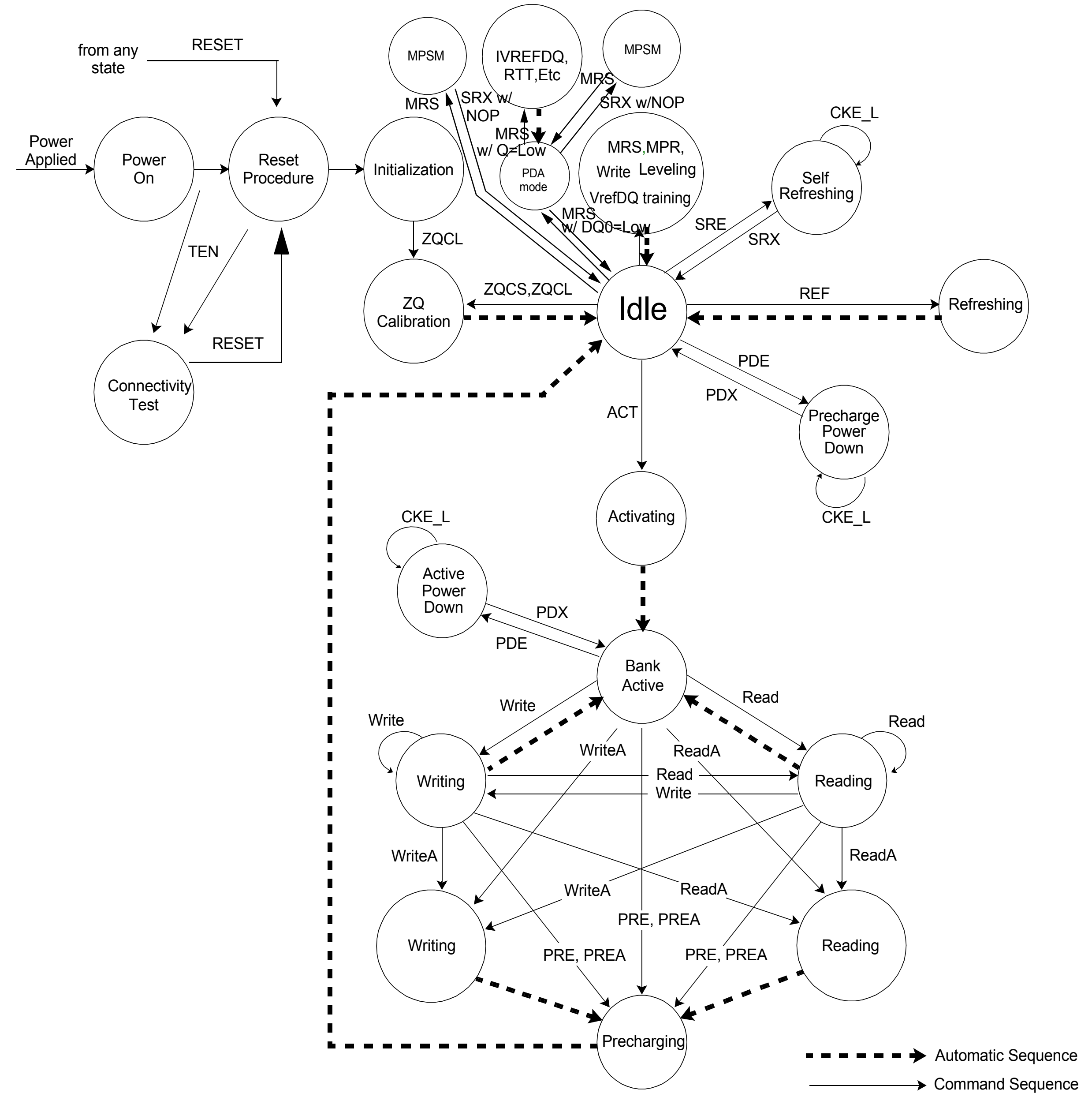
DDR4 SDRAM Specification

1. Functional Description

1.1 Simplified State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD,RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	PRECHARGE All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA,WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
REF	Refresh, Fine granularity Refresh	RESET_n	Start RESET procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

NOTE :
1. This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than on bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

1.2 Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM.

The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a ‘chopped’ burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to “DDR4 SDRAM Addressing” on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode ‘on the fly’ (via A12) if enabled in the mode register.

Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

1.3 RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly default values for the following MR settings need to be defined.

Gear down mode (MR3 A[3]) : 0 = 1/2 Rate

Per DRAM Addressability (MR3 A[4]) : 0 = Disable

Max Power Saving Mode (MR4 A[1]) : 0 = Disable

CS to Command/Address Latency (MR4 A[8:6]) : 000 = Disable

CA Parity Latency Mode (MR5 A[2:0]) : 000 = Disable

Post Package Repair mode (MR4 A[13]) : 0 = Disable

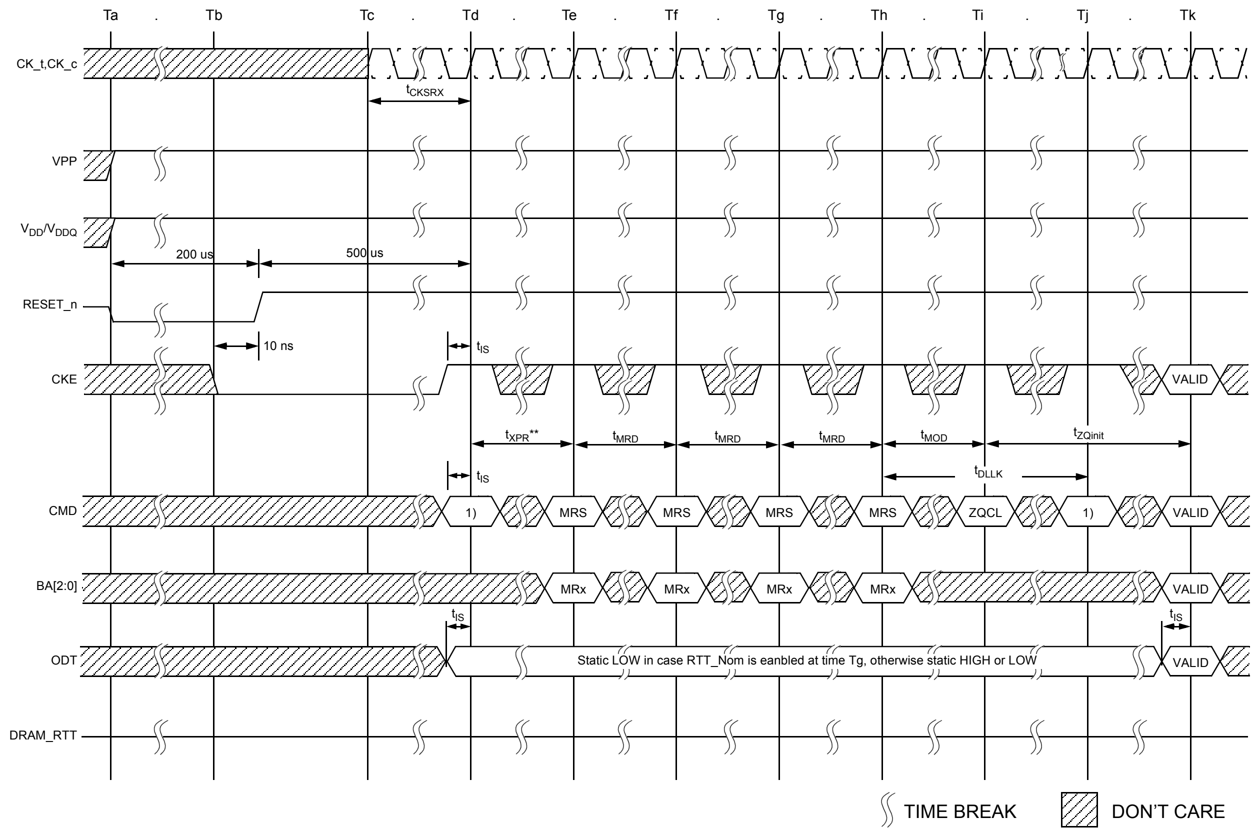
Target Row Refresh (MR2 A[13]) : 0 = Disable

1.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization and is shown in Figure 1.

1. Apply power (RESET_n is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained for minimum 200us with stable power. CKE is pulled " Low" anytime before RESET_n being de-asserted (min. time 10ns) . The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and (V_{DD}-V_{DDQ}) < 0.3volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.
   - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.76V max once power ramp is finished, AND
   - VrefCA tracks VDD/2.

   or
   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & VrefCA.
   - Apply VPP without any slope reversal before or at the same time as VDD.
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After RESET_n is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK_t,CK_c) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a Deselect command must be registered (with tIS set up time to clock) at clock edge Td. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit
4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as RESET_n is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET_n deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=Max(tXS, 5nCK)]
6. Issue MRS Command to to load MR3 with all application settings(To issue MRS command to MR3, provide " Low" to BG0, "High" to BA1, BA0)
7. Issue MRS command to load MR6 with all application settings (To issue MRS command to MR6, provide "Low" to BA0, "High" to BG0, BA1)
8. Issue MRS command to load MR5 with all application settings (To issue MRS command to MR5, provide "Low" to BA1, "High" to BG0, BA0)
9. Issue MRS command to load MR4 with all application settings (To issue MRS command to MR4, provide "Low" to BA1, BA0, "High" to BG0)
10. Issue MRS command to load MR2 with all application settings (To issue MRS command to MR2, provide "Low" to BG0, BA0, "High" to BA1)
11. Issue MRS command to load MR1 with all application settings (To issue MRS command to MR1, provide "Low" to BG0, BA1, "High" to BA0)
12. Issue MRS command to load MR0 with all application settings (To issue MRS command to MR0, provide "Low" to BG0, BA1, BA0)
13. Issue ZQCL command to starting ZQ calibration
14. Wait for both tDLLK and tZQ init completed
15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).



NOTE :
1. From time point 'Td' until 'Tk', DES commands must be applied between MRS and ZQCL commands.
2. MRS Commands must be issued to all Mode Registers that have defined settings.

Figure 1. RESET_n and Initialization Sequence at Power-on Ramping

1.3.2 VDD Slew rate at Power-up Initialization Sequence

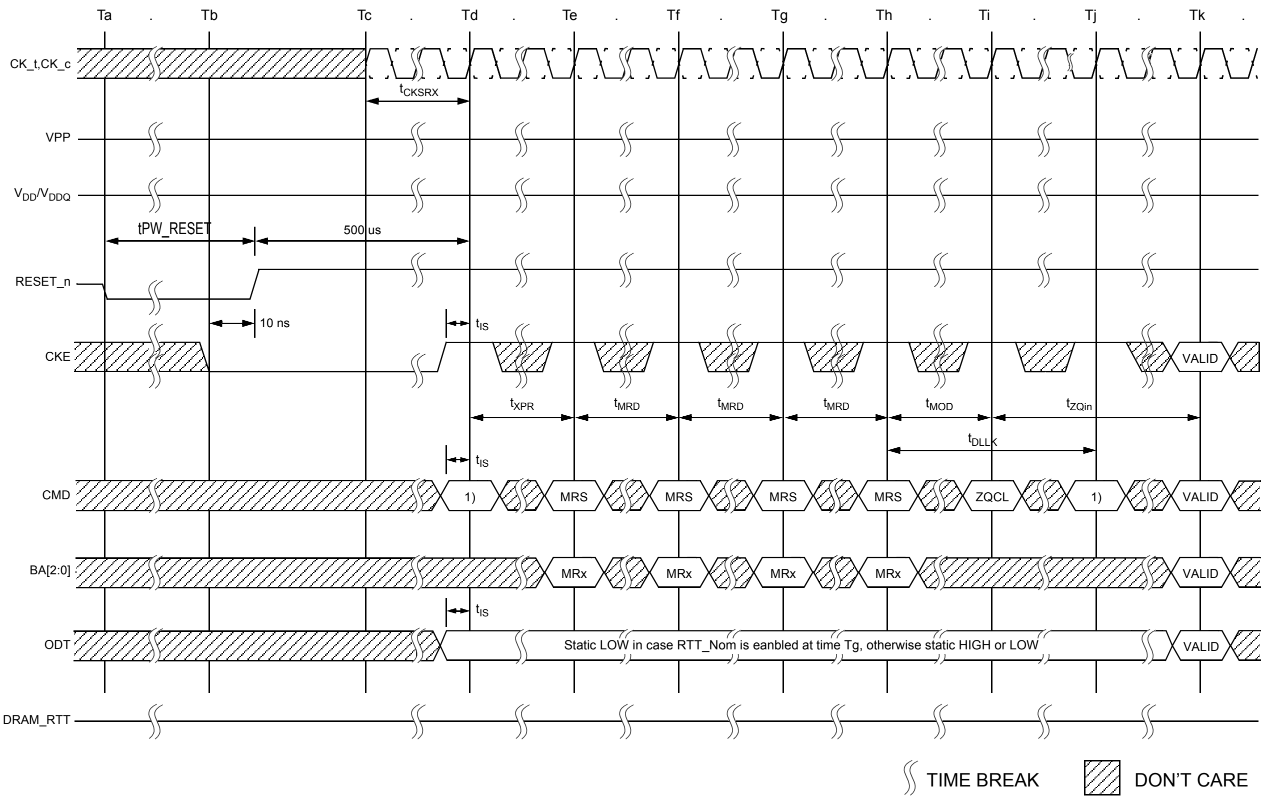
[Table 1] VDD Slew Rate

Symbol	Min	Max	Units
VDD_sl[1]	0.004	600	V/ms[2]
VDD_ona	0	200	ms[3]

1. Measurement made between 300mv and 80% Vdd minimum.
2. 20 MHz bandlimited measurement.
3. Maximum time to ramp VDD from 300 mv to VDD minimum.

1.3.3 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization as shown in Figure 2.
1. Asserted RESET_n below 0.2 * V_{DD} anytime when reset is needed (all other inputs may be undefined). RESET_n needs to be maintained for minimum tPW_RESET. CKE is pulled "LOW" before RESET_n being de-asserted (min. time 10 ns).
2. Follow steps 2 to 10 in "Power-up Initialization Sequence" on page 13.
3. The Reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include Vref training and Write leveling)



NOTE :

1. From time point 'Td' until 'Tk', DES commands must be applied between MRS and ZQCL commands
2. MRS Commands must be issued to all Mode Registers that have defined settings.

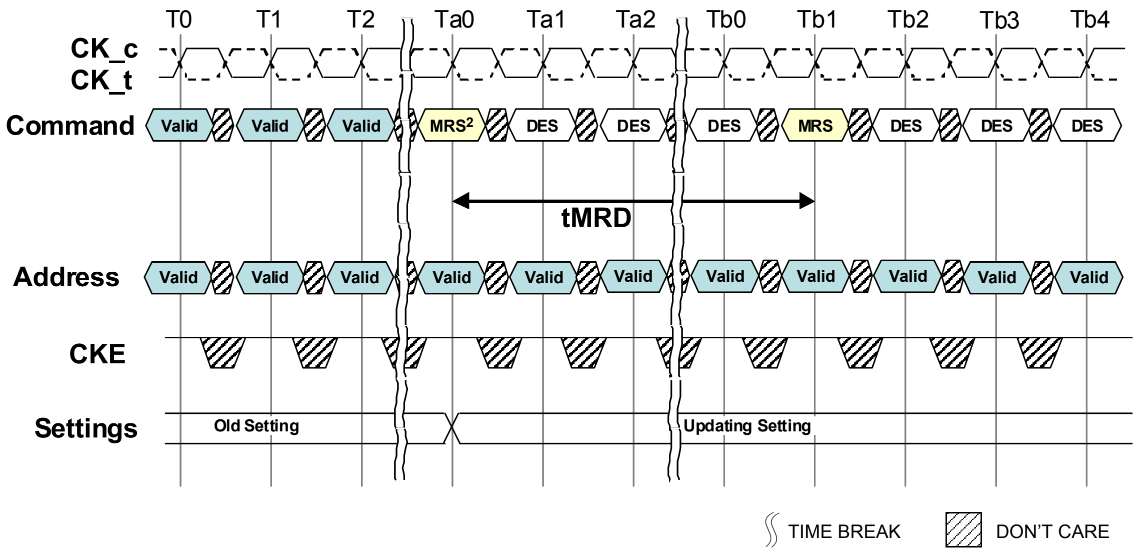
Figure 2. Reset Procedure at Power Stable

1.4 Register Definition

1.4.1 Programming the mode registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/ or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 3



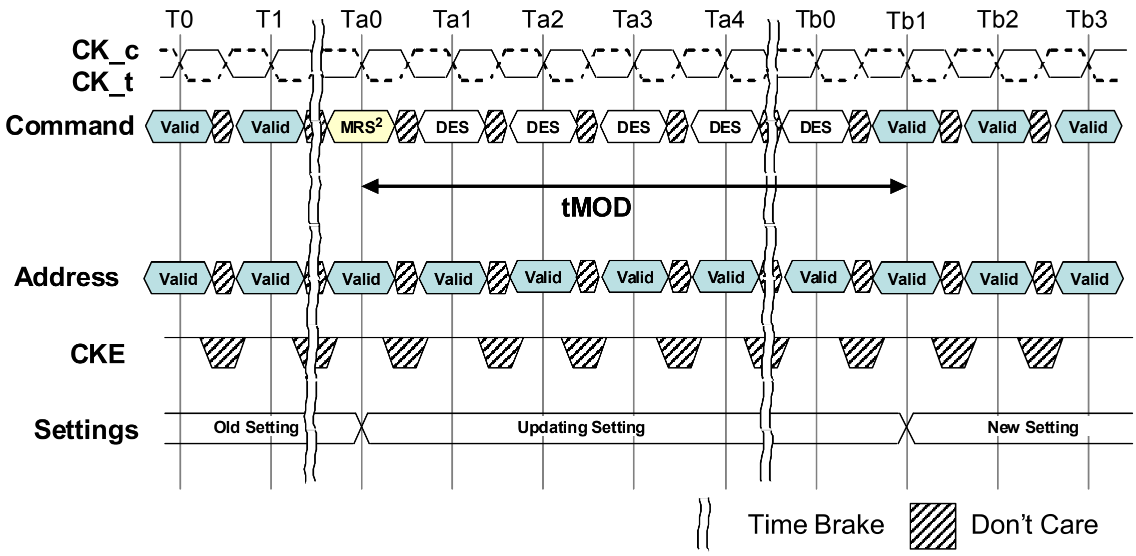
NOTE :
1. This timing diagram shows C/A Parity Latency mode is “Disable” case.
2. List of MRS commands exception that do not apply to tMRD
- Gear down mode
- C/A Parity Latency mode
- CS to Command/Address Latency mode
- Per DRAM Addressability mode
- VrefDQ training Value, VrefDQ Training mode and VrefDQ training Range

Figure 3. tMRD Timing

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.

This type of MRS command does not apply tMRD timing to next MRS command is listed in note 2 of Figure 3. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

The most MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding DES shown in Figure 4.



NOTE :

1. This timing diagram shows CA Parity Latency mode is “Disable” case.
2. List of MRS commands exception that do not apply to tMOD

- DLL Enable, DLL Reset
- VrefDQ training Value, internal Vref Monitor, VrefDQ Training mode and VrefDQ training Range
- Gear down mode
- Per DRAM addressability mode
- Maximum power saving mode
- CA Parity mode

Figure 4. tMOD Timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. For MRS command, If RTT_Nom function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring RTT_NOM is in an off state prior to MRS command affecting RTT_NOM turn-on and off timing. Refer to note2 of Figure 4 for this type of MRS. The ODT signal may be registered high after tMOD has expired. ODT signal is a don’t care during MRS command if DRAM RTT_Nom function is disabled in the mode register prior and after an MRS command.

Some of the mode register setting cases, function updating takes longer than tMOD. This type of MRS does not apply tMOD timing to next valid command excluding DES is listed in note 2 of Figure 4. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

1.5 Mode Register

MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13[5],A11:A9	WR and RTP[2, 3]	Write Recovery and Read to Precharge for auto precharge(see Table 2)
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A12,A6:A4,A2	CAS Latency[4]	(see Table 3)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

NOTE :
1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer:WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
3. The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
4. The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency. Cas Latency controlled by A12 is optional for 4Gb device.
5. A13 for WR and RTP setting is optional for 4Gb.

[Table 2] Write Recovery and Read to Precharge (cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

[Table 3] CAS Latency

	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25 (only 3DS available)
1	0	0	0	1	26
1	0	0	1	0	27 (only 3DS available)
1	0	0	1	1	28
1	0	1	0	0	reserved for 29
1	0	1	0	1	30
1	0	1	1	0	reserved for 31
1	0	1	1	1	32
1	1	0	0	0	reserved

MR1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[3]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff[1]	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see Table 4)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6, A5	RFU	0 = must be programmed to 0 during MRS
A4, A3	Additive Latency	00 = 0(AL disabled) 10 = CL-2 01 = CL-1 11 = Resrved
A2, A1	Output Driver Impedance Control	(see Table 5)
A0	DLL Enable	0 = Disable[2] 1 = Enable

NOTE :

1. Outputs disabled - DQs, DQS_ts, DQS_cs.
2. States reversed to "0 as Disable" with respect to DDR4.
3. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

[Table 4] RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

[Table 5] Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

MR2

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	TRR	0 = Disable 1 = Enable
A12	Write CRC	0 = Disable 1 = Enable
A11	RFU	0 = must be programmed to 0 during MRS
A11,A10:A9	RTT_WR	(see Table 6)
A8, A2	TRR Mode - BGn	00 = BG0 10 = BG2 01 = BG1 11 = BG3
A7:A6	Low Power Array Self Refresh (LP ASR)	00 = Manual Mode (Normal Operaing Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A5:A3	CAS Write Latency(CWL)	(see Table 7)
A1:A0	TRR Mode - BAn	00 = Bank 0 10 = Bank 2 01 = Bank 1 11 = Bank 3

NOTE :
1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

[Table 6] RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT Off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

[Table 7] CWL (CAS Write Latency)

A5	A4	A3	CWL	Speed Grade in MT/s for 1 tCK Write Preamble		Speed Grade in MT/s for 2 tCK Write Preamble [1]	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	3200	2400	2666	2400
1	1	0	18		2666	3200	2666
1	1	1	20		3200		3200

1. The 2 tCK Write Preamble is valid for DDR4-2400/2666/3200 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional CWL is needed.

MR3

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A11	MPR Read Format	00 = Serial 10 = Staggered 01 = Parallel 11 = ReservedTemperature
A10:A9	Write CMD Latency when CRC and DM are enabled	(see Table 9)
A8:A6	Fine Granularity Refresh Mode	(see Table 8)
A5	Temperature sensor readout	0 : disabled 1: enabled
A4	Per DRAM Addressability	0 = Disable 1 = Enable
A3	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A2	MPR Operation	0 = Normal 1 = Dataflow from/to MPR
A1:A0	MPR page Selection	00 = Page0 10 = Page2 01 = Page1 11 = Page3 (see Table.8)

NOTE :
1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

[Table 8] Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

[Table 9] MR3 A<10:9> Write Command Latency when CRC and DM are both enabled

A10	A9	CRC+DM Write Command Latency	Speed Bin
0	0	4nCK	1600
0	1	5nCK	1866,2133,2400
1	0	6nCK	TBD
1	1	RFU	RFU

[Table 10] MPR Data Format

MPR page0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page1 (CA Parity Error Log)

<table>
<tr><th>Address</th><th>MPR Location</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>note</th></tr>
<tr><td rowspan="5">BA1:BA0</td><td>00 = MPR0</td><td>A[7]</td><td>A[6]</td><td>A[5]</td><td>A[4]</td><td>A[3]</td><td>A[2]</td><td>A[1]</td><td>A[0]</td><td rowspan="5">Read-only</td></tr>
<tr><td>01 = MPR1</td><td>CAS_n/ A15</td><td>WE_n/ A14</td><td>A[13]</td><td>A[12]</td><td>A[11]</td><td>A[10]</td><td>A[9]</td><td>A[8]</td></tr>
<tr><td>10 = MPR2</td><td>PAR</td><td>ACT_n</td><td>BG[1]</td><td>BG[0]</td><td>BA[1]</td><td>BA[0]</td><td>A[17]</td><td>RAS_n/ A16</td></tr>
<tr><td rowspan="2">11 = MPR3</td><td rowspan="2">CRC Error Status</td><td rowspan="2">CA Parity Error Status</td><td colspan="3">CA Parity Latency^{4}</td><td rowspan="2">C[2]</td><td rowspan="2">C[1]</td><td rowspan="2">C[0]</td></tr>
<tr><td>MR5.A[2]</td><td>MR5.A[1]</td><td>MR5.A[0]</td></tr>
</table>

NOTE :

1. MPR used for C/A parity error log readout is enabled by setting A[2] in MR3
2. For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don’t care.
3. If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don’t care.
4. MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.

MPR page2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	PPR	RFU sPPR	RTT_WR	Temperature Sensor Status(Table1)		CRC Write Enable	Rtt_WR		read-only
		-	-	MR2	-	-	MR2	MR2		
		-	-	A11	-	-	A12	A10	A9	
	01= MPR1	Vref DQ Trng range	Vref DQ training Value						Gear-down Enable	
		MR6	MR6						MR3	
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	CAS Latency					CAS Write Latency			
		MR0					MR2			
		A6	A5	A4	A2	A12	A5	A4	A3	
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver Impedance		
		MR1			MR5			MR1		
		A10	A9	A6	A8	A7	A6	A2	A1	

MR bit for Temperature Sensor Readout
MR3 bit A5=1 : DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.
MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X refresh (> tREFI)
0	1	1X refresh rate(= tREFI)
1	0	2X refresh rate(1/2* tREFI)
1	1	rsvd

MPR page3 (Vendor use only)[1]

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	Read-only
	01 = MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	11 = MPR3	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	

NOTE :
1. MPR page3 is specifically assigned to DRAM. Actual encoding method is vendor specific.

MR4

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	PPR	0 = Disable 1 = Enable
A12	Write Preamble	0 = 1 nCK 1 = 2 nCK
A11	Read Preamble	0 = 1 nCK 1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable 1 = Enable
A9	Self Refresh Abort	0 = Disable 1 = Enable
A8:A6	CS to CMD/ADDR Latency Mode (cycles)	000 = Disable 100 = 6 001 = 3 101 = 8 010 = 4 110 = Reserved 011 = 5 111 = Reserved (See Table 11)
A5	RFU	0 = must be programmed to 0 during MRS
A4	Internal Vref Monitor	0 = Disable 1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable 1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A1	Maximum Power Down Mode	0 = Disable 1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS

NOTE :

1.Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

[Table 11] CS to CMD / ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

MR5

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	CA parity Persistent Error	0 = Disable1 = Enable
A8:A6	RTT_PARK	(see Table 12)
A5	ODT Input Buffer during Power Down mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A4	C/A Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2:A0	C/A Parity Latency Mode	(see Table 13)

NOTE :
1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

[Table 12] RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

[Table 13] C/A Parity Latency Mode

A2	A1	A0	PL	Speed Bin
0	0	0	Disable	
0	0	1	4	1600,1866,2133
0	1	0	5	2400
0	1	1	6	RFU
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

NOTE:
1. Parity latency must be programmed according to timing parameters by speed grade table

MR6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A10	tCCD_L	(see Table 14)
A9, A8	RFU	0 = must be programmed to 0 during MRS
A7	VrefDQ Training Enable	0 = Disable(Normal operation Mode) 1 = Enable(Training Mode)
A6	VrefDQ Training Range	(see Table 15)
A5:A0	VrefDQ Training Value	(see Table 16)

NOTE :
1.Reserved for Register control word setting . DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond.

[Table 14] tCCD_L & tDLLK

A12	A11	A10	tCCD_L.min (nCK)[1]	tDLLKmin (nCK)[1]	Note
0	0	0	4	597	Data rate ≤ 1333Mbps
0	0	1	5		1333Mbps < Data rate ≤ 1866Mbps (1600/ 1866Mbps)
0	1	0	6	768	1866Mbps < Data rate ≤ 2400Mbps (2133/ 2400Mbps)
0	1	1	7	1024	≤ TBD
1	0	0	8		≤ TBD
1	0	1	Reserved		
1	1	0			
1	1	1			

NOTE :
1. tCCD_L/tDLLK should be programmed according to the value defined in AC parameter table per operating frequency

[Table 15] VrefDQ Training : Range

A6	VrefDQ Range
0	Range 1
1	Range 2

[Table 16] VrefDQ Training : Values

A5:A0	Range1	Range2
00 0000	60.00%	45.00%
00 0001	60.65%	45.65%
00 0010	61.30%	46.30%
00 0011	61.95%	46.95%
00 0100	62.60%	47.60%
00 0101	63.25%	48.25%
00 0110	63.90%	48.90%
00 0111	64.55%	49.55%
00 1000	65.20%	50.20%
00 1001	65.85%	50.85%
00 1010	66.50%	51.50%
00 1011	67.15%	52.15%
00 1100	67.80%	52.80%
00 1101	68.45%	53.45%
00 1110	69.10%	54.10%
00 1111	69.75%	54.75%
01 0000	70.40%	55.40%
01 0001	71.05%	56.05%
01 0010	71.70%	56.70%
01 0011	72.35%	57.35%
01 0100	73.00%	58.00%
01 0101	73.65%	58.65%
01 0110	74.30%	59.30%
01 0111	74.95%	59.95%
01 1000	-75.60%	60.60%
01 1001	76.25%	61.25%
01 1010	76.90%	61.90%
01 1011	77.55%	62.55%
01 1100	78.20%	63.20%
01 1101	78.85%	63.85%
01 1110	79.50%	64.50%
01 1111	80.15%	65.15%
10 0000	80.80%	65.80%
10 0001	81.45%	66.45%
10 0010	82.10%	67.10%
10 0011	82.75%	67.75%
10 0100	83.40%	68.40%
10 0101	84.05%	69.05%
10 0110	84.70%	69.70%
10 0111	85.35%	70.35%
10 1000	86.00%	71.00%
10 1001	86.65%	71.65%
10 1010	87.30%	72.30%
10 1011	87.95%	72.95%
10 1100	88.60%	73.60%
10 1101	89.25%	74.25%
10 1110	89.90%	74.90%
10 1111	90.55%	75.55%
11 0000	91.20%	76.20%
11 0001	91.85%	76.85%
11 0010	92.50%	77.50%
11 0011 to 11 1111	Reserved	Reserved

DRAM MR7 Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM.Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

1.6 3DS Functional Description

1.6.1 Simplified State Diagram

There is no difference between the simplified state diagrams for DDR4 and 3DS DDR4. Situations involving more than one bank, and multiple logical ranks are not reflected in the simple state diagram for DDR4 and are not captured in full detail.

1.6.2 Basic Functionality

The 3DS DDR4 SDRAM is a 2H, 4H or 8H stacked high-speed dynamic random-access memory with each logical rank configured as a 16-bank SDRAM (organized into four bank groups of four banks each). The 3DS SDRAM has 32, 64 or 128 physical banks available internally, depending on the number of logical ranks. The 3DS DDR4 SDRAM retains the use of an 8n pre-fetch architecture to achieve highspeed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the 3DS DDR4 SDRAM consists of a single 8n-bit wide, one clock data transfer at the internal SDRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

1.6.3 Reset Signal and Initialization Procedure

Prior to normal operation, the 3DS DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation. A single reset pin with a single load is available per 3DS device. It is expected that the entire stack of SDRAMs within the package reset as per DDR4 specification. After RESET_n is de-asserted, the SDRAM will start internal state initialization; this will be done independently of external clocks. All steps in the DDR4 initialization sequence must be followed. No additional steps are required for 3DS DDR4 devices but the unique nature of 3DS devices (which have a single external I/O structure shared by all logical ranks of the entire device) has to be considered when programing the SDRAM mode register bits (see next section for details).

1.6.4 Mode Register Definition

For application flexibility, various functions, features and modes are programmable in seven Mode Registers. One set of registers controls the entire stack regardless if the 3DS stack has two, four or eight logical ranks, and they must be programmed via a Mode Register Set (MRS) command. For 3DS DDR4 stacks configured as n logical ranks, a single set of MRS registers is addressed by the Chip Select signal (CS_n)as shown in Table 17.

[Table 17] Simplified Truth Table for MRS Command

DRAM Command	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	Notes
Mode Register Set	L	V	V	V	MRS	MRS	MRS	MRS	MRS	MRS	MRS	MRS	1.2
Mode Register Set	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	2
Any other command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	2

Programming the register fields for a stacked device has some special considerations. Waiting for tMRD is required between two MRS commands issued to a 3DS SDRAM. After an MRS command is given, waiting for tMOD is required before a non-MRS command can be issued to any of the logical ranks in the stack. Due to the difference between CAS Latency and nRCD, DDR4 3DS devices require a different Additive Latency definition than mono DDR4 SDRAMs.

MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A11:A9	WR and RTP[2, 3]	Write Recovery and Read to Precharge for auto precharge(see Table 18)
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A12,A6:A4,A2	CAS Latency[4]	(see Table 19, “CAS Latency”)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

NOTE :

1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer:WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
3. The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
4. The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency which device supports. A12 is an additional bit to encode for Cas Latency. Hence availability of A12=1 could depend on Device.

[Table 18] Write Recovery and Read to Precharge (cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

[Table 19] CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25 (only 3DS available)
1	0	0	0	1	26
1	0	0	1	0	27 (only 3DS available)
1	0	0	1	1	28
1	0	1	0	0	reserved for 29
1	0	1	0	1	30
1	0	1	1	0	reserved for 31
1	0	1	1	1	32
1	1	0	0	0	reserved

MR1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[3]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff[1]	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see Table 20)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6, A5	RFU	0 = must be programmed to 0 during MRS
A4, A3	Additive Latency[4]	00 = 0(AL disabled) 10 = CL-2 01 = Reserved 11 = CL-3
A2, A1	Output Driver Impedance Control	(see Table 21)
A0	DLL Enable	0 = Disable[2] 1 = Enable

NOTE :
1. Outputs disabled - DQs, DQS_ts, DQS_cs.
2. States reversed to “0 as Disable” with respect to DDR4.
3. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.
4. When the gap between tAA and tRCD is bigger than 2 clock cycles, host should increment tRCD accordingly to use AL, knowing that DDR4 3DS only supports AL of CL-2 and CL-3.

[Table 20] RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

[Table 21] Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

MR2

Address	Operating Mode	Description
C2, C1, C0	TRR Mode Chip ID	000 = LR0 100 = LR4 001 = LR1 101 = LR5 010 = LR2 110 = LR6 011 = LR3 111 = LR7
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	TRR	0 = Disable 1 = Enable
A12	Write CRC	0 = Disable 1 = Enable
A11	RFU	0 = must be programmed to 0 during MRS
A11,A10:A9	RTT_WR	(see Table 22)
A8, A2	TRR Mode - BGn	00 = BG0 10 = BG2 01 = BG1 11 = BG3
A7:A6	Low Power Array Self Refresh (LP ASR)	00 = Manual Mode (Normal Operaing Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A5:A3	CAS Write Latency(CWL)	(see Table 23)
A1:A0	TRR Mode - BAn	00 = Bank 0 10 = Bank 2 01 = Bank 1 11 = Bank 3

NOTE :
1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

[Table 22] RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT Off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

[Table 23] CWL (CAS Write Latency)

A5	A4	A3	CWL	Speed Grade in MT/s for 1 tCK Write Preamble		Speed Grade in MT/s for 2 tCK Write Preamble [1]	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	3200	2400	2666	2400
1	1	0	18		2666	3200	2666
1	1	1	20		3200		3200

1. The 2 tCK Write Preamble is valid for DDR4-2400/2666/3200 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional CWL is needed.

2. DDR4 SDRAM Command Description and Operation

2.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write commands.
[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

[Table 24] Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	BG0-BG1	BA0-BA1	C2-C0	A12/BC_n	A17, A13, A11	A10/AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address(RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

NOTE :
1. All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependant. When ACT_n = H; pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n respectively. When ACT_n = L; pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as address pins A16, A15, and A14 respectively
2. RESET_n is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3 Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Controller guarantees self refresh exit to be synchronous.
9. VPP and VREF(VrefCA) must be maintained during Self Refresh operation.
10. The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit
11. Refer to the CKE Truth Table for more detail with CKE transition.
12. During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

2.2 CKE Truth Table

[Table 25] CKE Truth Table

Current State[2]	CKE Previous Cycle[1] (N-1)	CKE Current Cycle[1] (N)	Command (N)[3] RAS_n, CAS_n, WE_n, CS_n	Action (N)[3]	NOTE
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See “Command Truth Table”.					10

NOTE :
1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are DESELECT only.
12. Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.
13. Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See “Self-Refresh Operation” on Section 2.27 and See “Power-Down Modes” on Section 2.28.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VPP and VREF(VrefCA) must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP,etc)

2.3 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 of Mode Register MR0. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 18. The burst length is defined by bits A0-A1 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC_n.

[Table 26] Burst Type and Burst Order

Burst Length	Read/Write	Starting Column Address (A2,A1,A0)	burst type = Sequential (decimal) A3=0	burst type = Interleaved (decimal) A3=1	NOTE
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1,2,3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1,2,3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1,2,3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1,2,3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1,2,3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1,2,3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1,2,3
	WRITE	0, V, V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1, V, V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1,2,4,5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V, V, V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

NOTE :
1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC_n, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. Output driver for data and strobes are in high impedance.
4. V : A valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X : Don't Care.

2.3.1 BL8 Burst order with CRC Enabled

DDR4 SDRAM supports fixed write burst ordering [A2:A1:A0=0:0:0] when write CRC is enabled in BL8 (fixed).

2.4 DLL-off Mode & DLL on/off Switching procedure

2.4.1 DLL on/off switching procedure

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”.

2.4.2 DLL “on” to DLL “off” Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT_NOM, must be in high impedance state before MRS to MR1 to disable the DLL.)

2. Set MR1 bit A0 to “0” to disable the DLL.

3. Wait tMOD.

4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.

5. Change frequency, in guidance with “Input clock frequency change” on Section 2.6.

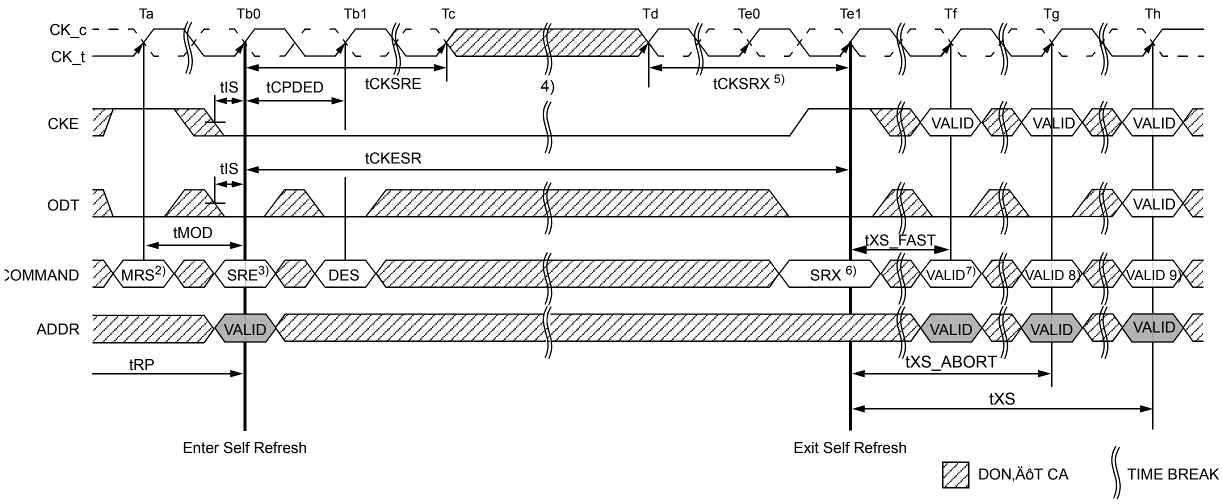
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.

7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If RTT_NOM features were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don’t Care.

8. Wait tXS_Fast or tXS_Abort or tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS_Fast).

- tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8
- tXS_Fast - ZQCL, ZQCS, MRS commands. For MRS command, only DRAM CL and WR/RTP register in MR0, CWL register in MR2 and geardown mode in MR3 are allowed to be accessed provided DRAM is not in per DRAM addressibility mode. Access to other DRAM mode registers must satisfy tXS timing.
- tXS_Abort - If the MR4 bit A9 is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of tXS_abort. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

9. Wait for tMOD, then DRAM is ready for next command.



1. Starting with Idle State, RTT in Stable
2. Disable DLL by setting MR1 Bit A0 to 0
3. Enter SR
4. Change Frequency
5. Clock must be stable tCKSRX
6. Exit SR
7.8.9. Update Mode registers allowed with DLL off parameters setting

Figure 5. DLL Switch Sequence from DLL ON to DLL OFF

2.4.3 DLL “off” to DLL “on” Procedure

To switch from DLL “off” to DLL “on” (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT_NOM) must be in high impedance state before Self-Refresh mode is entered.)

2. Enter Self Refresh Mode, wait until tCKSRE satisfied.

3. Change frequency, in guidance with "Input clock frequency change" on Section 2.6.

4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.

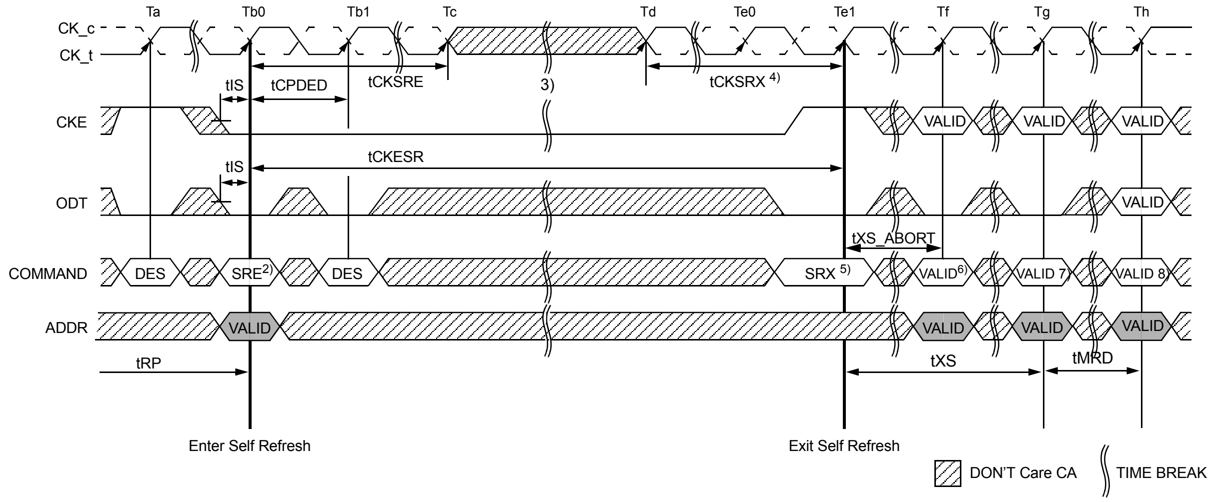
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If RTT_NOM were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don’t care.

6. Wait tXS or tXS_ABORT depending on Bit A9 in MR4, then set MR1 bit A0 to “1” to enable the DLL.

7. Wait tMRD, then set MR0 bit A8 to “1” to start DLL Reset.

8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)

9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.



1. Starting with Idle State
2. Enter SR
3. Change Frequency
4. Clock must be stable tCKSRX
5. Exit SR
6.7. Set DLL-on by MR1 A0='1'
8. Start DLLReset
9. Update rest MR register values after tDLLK (not shown in the diagram)
10. Ready for valid command after tDLLK (not shown in the diagram)

Figure 6. DLL Switch Sequence from DLL OFF to DLL ON

2.5 DLL-off Mode

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to “Input clock frequency change” on Section 2.6.

The DLL-off Mode operations listed below are an optional feature for DDR4 SDRAM. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=10 and CWL=9. When DLL-off Mode is enabled, use of CA Parity Mode is not allowed.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command.
Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.
tDQSCK(DLL_off) values are vendor specific.
The timing relations on DLL-off mode READ operation are shown in the following Timing Diagram
(CL=10, BL=8, PL=0):

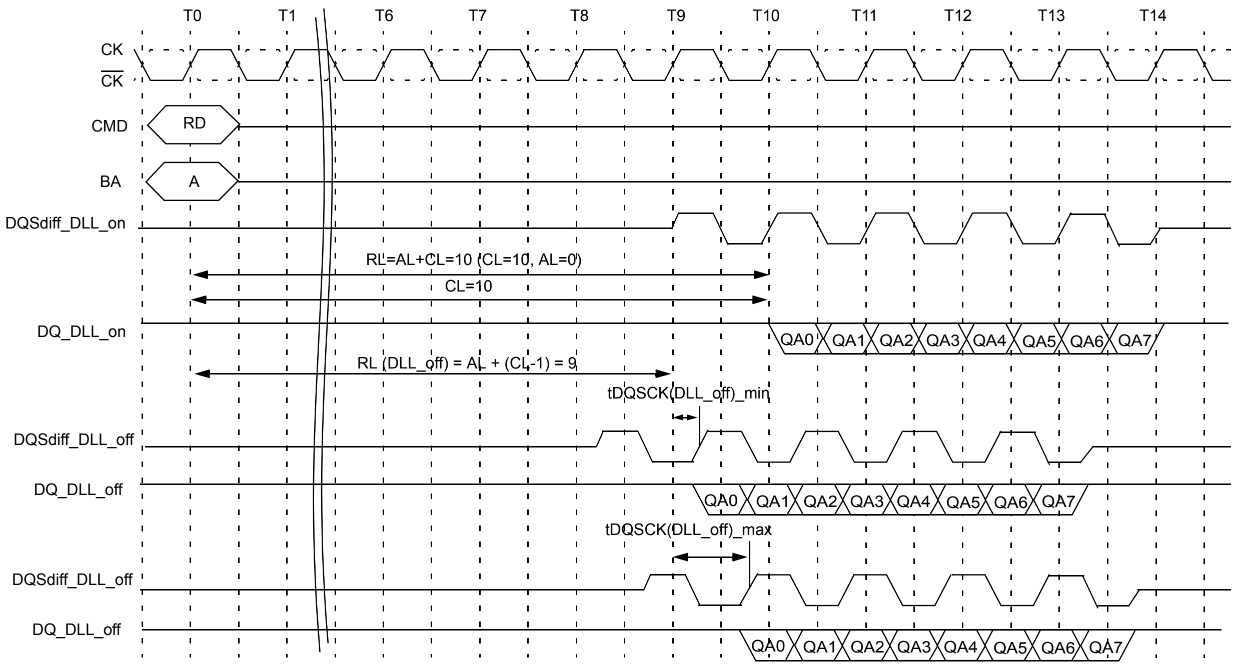


Figure 7. READ operation at DLL-off mode

2.6 Input Clock Frequency Change

Once the DDR4 SDRAM is initialized, the DDR4 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under Self-Refresh mode . Outside Self-Refresh mode, it is illegal to change the clock frequency.
Once the DDR4 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in Section 2.27 “Self-Refresh Operation”.
For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4 and MR6 may need to be issued to program appropriate CL, CWL, geardown mode, Read & Write Preamble and tCCD_L/tDLLK value. If MR6 is issued prior to Self Refresh Entry for new tDLLK value, then DLL will relock automatically at Self Refresh Exit. However, if MR6 is issued after Self Refresh Entry, then MR0 must be issued to reset the DLL.
The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to “DLL on/off switching procedure” on Section 2.4.

2.7 Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR4 SDRAM supports a ‘write leveling’ feature to allow the controller to compensate for skew. This feature may not be required under some system conditions provided the host can maintain the tDQSS, tDSS and tDSH specifications.

The memory controller can use the ‘write leveling’ feature and feedback from the DDR4 SDRAM to adjust the DQS_t - DQS_c to CK_t - CK_c relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS_t - DQS_c to align the rising edge of DQS_t - DQS_c with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK_t - CK_c, sampled with the rising edge of DQS_t - DQS_c, through the DQ bus. The controller repeatedly delays DQS_t - DQS_c until a transition from 0 to 1 is detected. The DQS_t - DQS_c delay established through this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS_t - DQS_c signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 8.

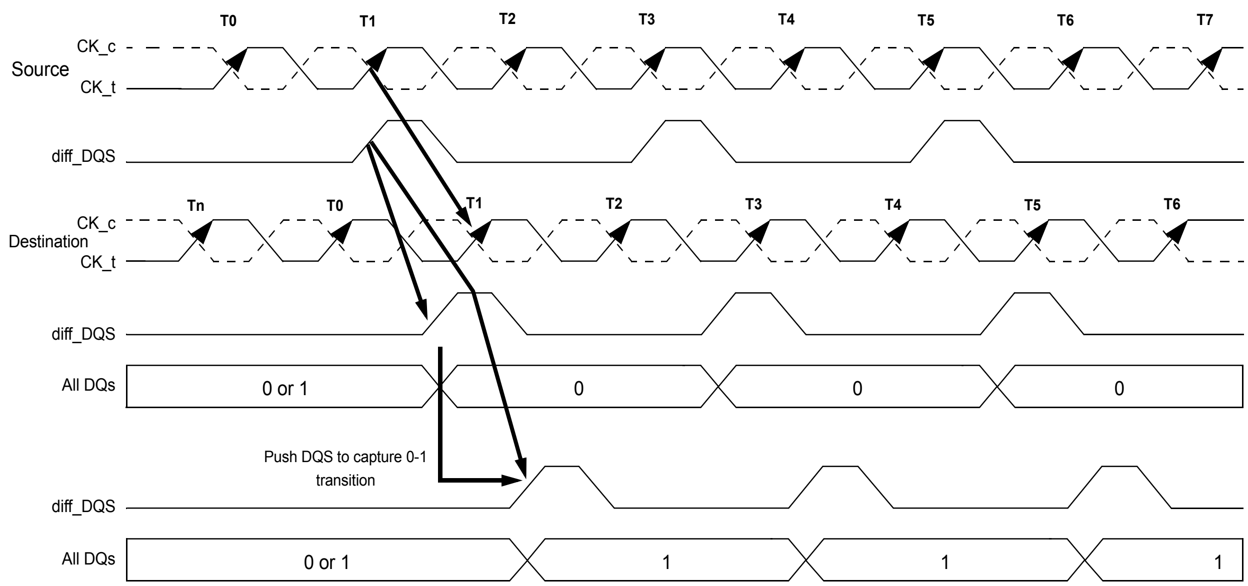


Figure 8. Write Leveling Concept

DQS_t - DQS_c driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

2.7.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set ’High’ and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set ’Low’ (Table 20). Note that in write leveling mode, only DQS_t/DQS_c terminations are activated and deactivated via ODT pin, unlike normal operation (Table 21).

[Table 27] MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

[Table 28] DRAM termination function in the leveling mode

ODT pin @DRAM if RTT_NOM/PARK Value is set via MRS	DQS_t/DQS_c termination	DQs termination
RTT_NOM with ODT High	On	Off
RTT_PARK with ODT LOW	On	Off

NOTE:

1. In Write Leveling Mode with its output buffer disabled (MR1[bit A7] = 1 with MR1[bit A12] = 1) all RTT_NOM and RTT_PARK settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit A7] = 1 with MR1[bit A12] = 0) all RTT_NOM and RTT_PARK settings are allowed.
2. Dynamic ODT function is not available in Write Leveling Mode. DRAM MR2 bits A[11:9] must be ‘000’ prior to entering Write Leveling Mode.

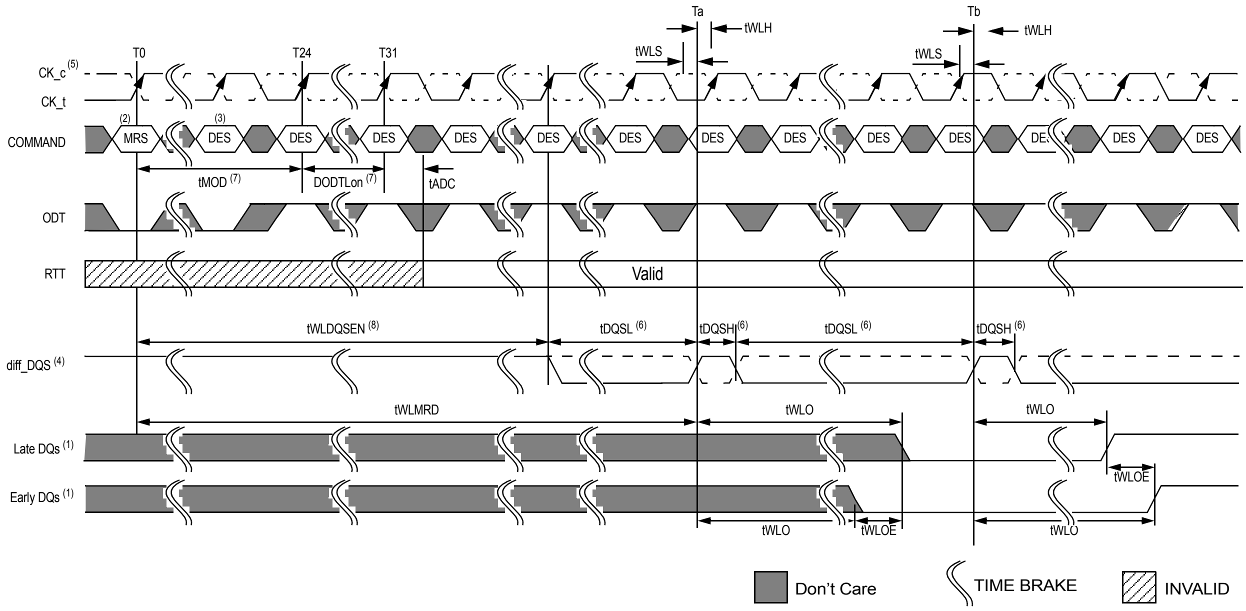
2.7.2 Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A8 ,A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS_t low and DQS_c high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS_t, DQS_c edge which is used by the DRAM to sample CK_t - CK_c driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK_t - CK_c status with rising edge of DQS_t - DQS_c and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS_t/DQS_c) needed for these DQs. Controller samples incoming DQs and decides to increment or decrement DQS_t - DQS_c delay setting and launches the next DQS_t/DQS_c pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS_t - DQS_c delay setting and write leveling is achieved for the device. Figure 9 describes the timing diagram and parameters for the overall Write Leveling procedure.

Parameter	Symbol	DDR4-1600,1866,2133,2400		DDR4-2666,3200		Units	NOTE
		Min	Max	Min	Max		
Write leveling output error	tWLOE	0	2	0	2	ns	



NOTE :

1. DDR4 SDRAM drives leveling feedback on all DQs
2. MRS : Load MR1 to enter write leveling mode
3. DES : Deselect
4. diff_DQS is the differential data strobe (DQS_t-DQS_c). Timing reference points are the zero crossings. DQS_t is shown with solid line, DQS_c is shown with dotted line
5. CK_t/CK_c : CK_t is shown with solid dark line, where as CK_c is drawn with dotted line.
6. DQS_t, DQS_c needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent
7 tMOD(Min) = max(24nCK, 15ns), WL = 9 (CWL = 9, AL = 0, PL = 0), DODTLon = WL -2 = 7
8 tWLDQSEN must be satisfied following equation when using ODT.
   - tWLDQSEN > tMOD(Min) + ODTLon + tADC : at DLL = Enable
   - tWLDQSEN > tMOD(Min) + tAONAS : at DLL = Disable

Figure 9. Timing details of Write leveling sequence [DQS_t - DQS_c is capturing CK_t - CK_c low at Ta and CK_t - CK_c high at Tb

2.7.3 Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MRS command (Te1).
2. Drive ODT pin low (tIS must be satisfied) and continue registering low. (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command may be registered. (MRS commands may be issued after tMRD (Td1).

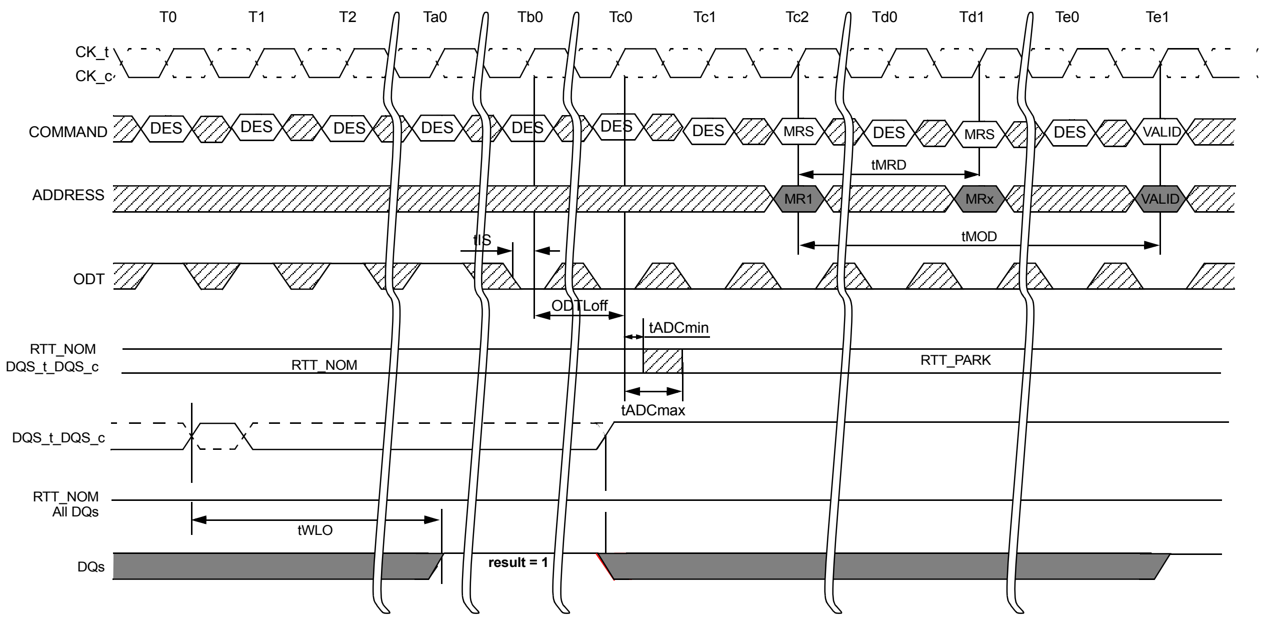


Figure 10. Timing details of Write leveling exit

2.8 Temperature controlled Refresh modes

This mode is enabled and disabled by setting bit A3 in MR4. Two modes are supported that are selected by bit A2 setting in MR4.

2.8.1 Normal temperature mode (0°C =< TCASE =< 85°C)

Once this mode is enabled by setting bit A3=1 and A2=0 in MR4, Refresh commands should be issued to DDR4 SDRAM with the Average periodic refresh interval (7.8us for 2Gb, 4Gb and 8Gb device, TBD for 16Gb device) which is tREFI of normal temperature range (0°C - 85°C). In this mode, the system guarantees that the DRAM temperature does not exceed 85°C.

Below 45°C, DDR4 SDRAM may adjust internal Average periodic refresh interval by skipping external refresh commands with proper gear ratio. Not more than three fourths of external refresh commands are skipped at any temperature in this mode.The internal Average periodic refresh interval adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

2.8.2 Extended temperature mode (0°C =< TCASE =< 95°C)

Once this mode is enabled by setting bit A3=1 and A2=1 in MR4, Refresh commands should be issued to DDR4 SDRAM with the Average periodic refresh interval (3.9 us for 2Gb, 4Gb and 8Gb device, TBD for 16Gb device) which is tREFI of extended temperature range (85°C - 95°C). In this mode, the system guarantees that the DRAM temperature does not exceed 95°C.

In the normal temperature range (0°C - 85°C), DDR4 SDRAM adjusts its internal Average periodic refresh interval to tREFI of the normal temperature range by skipping external refresh commands with proper gear ratio. Below 45°C, DDR4 SDRAM may further adjust internal Average periodic refresh interval . Not more than seven eighths of external commands are skipped at any temperature in this mode. The internal Average periodic refresh interval adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

2.9 Fine Granularity Refresh Mode

2.9.1 Mode Register and Command Truth Table

The Refresh cycle time (tRFC) and the average Refresh interval (tREFI) of DDR4 SDRAM can be programmed by MRS command. The appropriate setting in the mode register will set a single set of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device (fixed mode), or allow the dynamic selection of one of two sets of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device(on-the-fly mode). The on-the-fly mode must be enabled by MRS as shown in Table 22 before any on-the-fly- Refresh command can be issued.

[Table 29] MR3 definition for Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

There are two types of on-the-fly modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two on-the-fly modes is selected (‘A8=1’), DDR4 SDRAM evaluates BG0 bit when a Refresh command is issued, and depending on the status of BG0, it dynamically switches its internal Refresh configuration between 1x and 2x (or 1x and 4x) modes, and executes the corresponding Refresh operation. The command truth table is as shown in Table 23.

[Table 30] Refresh command truth table

<table>
<tr><th>Function</th><th>CS_n</th><th>ACT_n</th><th>RAS_n
/A16</th><th>CAS_n
/A15</th><th>WE_n
/A14</th><th>BG1</th><th>BG0</th><th>BA0-1</th><th>A10/
AP</th><th>A0-9,
A11-12,
A16-20</th><th>MR3 Setting</th></tr>
<tr><td>Refresh
(Fixed rate)</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td><td>A8 = ‘0’</td></tr>
<tr><td>Refresh
(on-the-fly 1x)</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>V</td><td>L</td><td>V</td><td>V</td><td>V</td><td>A8 = ‘1’</td></tr>
<tr><td>Refresh
(on-the-fly 2x)</td><td rowspan="2">L</td><td rowspan="2">H</td><td rowspan="2">L</td><td rowspan="2">L</td><td rowspan="2">H</td><td rowspan="2">V</td><td rowspan="2">H</td><td rowspan="2">V</td><td rowspan="2">V</td><td rowspan="2">V</td><td>A8:A7:A6=‘10 1’</td></tr>
<tr><td>Refresh
(on-the-fly 4x)</td><td>A8:A7:A6=‘11 0’</td></tr>
</table>

2.9.2 tREFI and tRFC parameters

The default Refresh rate mode is fixed 1x mode where Refresh commands should be issued with the normal rate, i.e. tREFI1 = tREFI(base) (for Tcase<=85°C), and the duration of each refresh command is the normal refresh cycle time (tRFC1). In 2x mode (either fixed 2x or on-the-fly 2x mode), Refresh commands should be issued to the DRAM at the double frequency (tREFI2 = tREFI(base)/2) of the normal Refresh rate. In 4x mode, Refresh command rate should be quadrupled (tREFI4 = tREFI(base)/4). Per each mode and command type, tRFC parameter has different values as defined in Table 24 .

The refresh command that should be issued at the normal refresh rate and has the normal refresh cycle duration may be referred to as a REF1x command. The refresh command that should be issued at the double frequency (tREFI2 = tREFI(base)/2) may be referred to as a REF2x command. Finally, the refresh command that should be issued at the quadruple rate (tREFI4 = tREFI(base)/4) may be referred to as a REF4x command.

In the Fixed 1x Refresh rate mode, only REF1x commands are permitted. In the Fixed 2x Refresh rate mode, only REF2x commands are permitted. In the Fixed 4x Refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x Refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the on-the-fly 1x/4x Refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

[Table 31] tREFI and tRFC parameters

Refresh Mode	Parameter		2Gb	4Gb	8Gb	16Gb	Unit
	tREFI(base)		7.8	7.8	7.8	TBD	us
1X mode	tREFI1	0°C <= TCASE <= 85°C	tREFI(base)	tREFI(base)	tREFI(base)	tREFI(base)	us
		85°C < TCASE <= 95°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	us
	tRFC1(min)		160	260	350	TBD	ns
2X mode	tREFI2	0°C <= TCASE <= 85°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	us
		85°C < TCASE <= 95°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	us
	tRFC2(min)		110	160	260	TBD	ns
4X mode	tREFI4	0°C <= TCASE <= 85°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	us
		85°C < TCASE <= 95°C	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	us
	tRFC4(min)		90	110	160	TBD	ns

2.9.3 Changing Refresh Rate

If Refresh rate is changed by either MRS or on the fly, new tREFI and tRFC parameters would be applied from the moment of the rate change. As shown in Figure 11, when REF1x command is issued to the DRAM, then tREF1 and tRFC1 are applied from the time that the command was issued. And then, when REF2x command is issued, then tREF2 and tRFC2 should be satisfied.

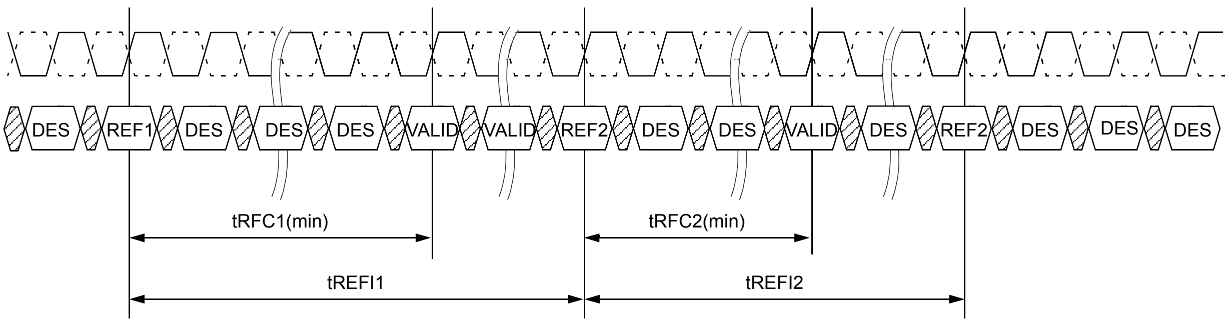


Figure 11. On-the-fly Refresh Command Timing

The following conditions must be satisfied before the Refresh rate can be changed. Otherwise, data retention of DDR4 SDRAM cannot be guaranteed.

1. In the fixed 2x Refresh rate mode or the on-the-fly 1x/2x Refresh mode, an even number of REF2x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate mode with an MRS command before the Refresh rate can be changed by another MRS command.
2. In the on-the-fly 1x/2x Refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.
3. In the fixed 4x Refresh rate mode or the on-the-fly 1x/4x Refresh mode, a multiple of-four number of REF4x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate with an MRS command before the Refresh rate can be changed by another MRS command.
4. In the on-the-fly 1x/4x Refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x Refresh rate mode. Switching between fixed and on-the-fly modes keeping the same rate is not regarded as a Refresh rate change.

2.9.4 Usage with Temperature Controlled Refresh mode

If the Temperature Controlled Refresh mode is enabled, then only the normal mode (Fixed 1x mode; A8:A7:A6='000') is allowed. If any other Refresh mode than the normal mode is selected, then the temperature controlled Refresh mode must be disabled.

2.9.5 Self Refresh entry and exit

DDR4 SDRAM can enter Self Refresh mode anytime in 1x, 2x and 4x mode without any restriction on the number of Refresh commands that has been issued during the mode before the Self Refresh entry. However, upon Self Refresh exit, extra Refresh command(s) may be required depending on the condition of the Self Refresh entry. The conditions and requirements for the extra Refresh command(s) are defined as follows

1. There are no special restrictions on the fixed 1x Refresh rate mode.
2. In the fixed 2x Refresh rate mode or the enable-on-the-fly 1x/2x Refresh rate mode, it is recommended that there should be an even number of REF2x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI).
3. In the fixed 4x Refresh rate mode or the enable-on-the-fly 1x/4x Refresh rate mode, it is recommended that there should be a multiple-of-four number of REF4x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or four extra REF4x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI).

2.10 Multi Purpose Register

2.10.1 DQ Training with MPR

The DDR4 DRAM contains four 8bit programmable MPR registers used for DQ bit pattern storage. These registers once programmed are activated with MRS read commands to drive the MPR bits on to the DQ bus during link training.

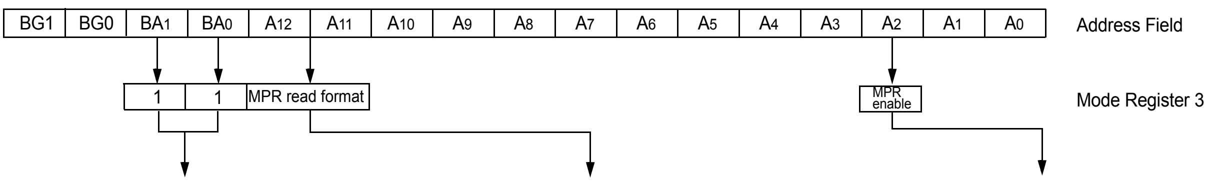
And DDR4 SDRAM only supports following command, MRS, RD, RDA WR, WRA, DES, REF and Reset during MPR enable Mode: MR3 [A2 = 1]. Note that in MPR mode RDA/WRA has the same functionality as a READ/WRITE command which means the auto precharge part of RDA/WRA is ignored. Power-Down mode and Self-Refresh command also is not allowed during MPR enable Mode. No other command can be issued within tRFC after REF command and 1x Refresh is only allowed when MPR mode is Enable. During MPR operations, MPR read or write sequence must be complete prior to a refresh command.

2.10.2 MR3 definition

Mode register MR3 controls the Multi-Purpose Registers (MPR) used for training. MR3 is written by asserting CS_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 low, ACT_n, BA0 and BA1 high and BG1[1] and BG0 low while controlling the states of the address pins according to the table below.

NOTE 1. x4/x8 only

MR3 Programming:



BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	A11	MPR read format
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

A2	MPR Operation
0	Normal operation
1	Dataflow from/to MPR

Read or Write with MPR LOCATION :

BA1	BA0	MPR Page Selection
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Default value for MPR0 @ Page0 = 01010101
Default value for MPR1 @ Page0 = 00110011
Default value for MPR2 @ Page0 = 00001111
Default value for MPR3 @ Page0 = 00000000

2.10.3 MPR Reads

MPR reads are supported using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR reads.

In MPR Mode:

Reads (back-to-back) from Page 0 may use tCCD_S or tCCD_L timing between read commands; Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between read commands; tCCD_L must be used for timing between read commands

MPR reads using BC4:

BA1 and BA0 indicate the MPR location within the selected page in MPR Mode.

A10 and other address pins are don't care including BG1 and BG0.
Read commands for BC4 are supported with starting column address of A2:A0 of '000' and '100'.

Data Bus Inversion (DBI) is not allowed during MPR Read operation.During MPR Read, DRAM ignores Read DBI Enable setting in MR5 bit A12 in MPR mode.

DDR4 MPR mode is enabled by programming bit A2=1 and then reads are done from a specific MPR location.
MPR location is specified with the Read command using Bank address bits BA1 and BA0.

Each MPR location is 8 bit wide.

STEPS:
DLL must be locked prior to MPR Reads. If DLL is Enabled : MR1[A0 = 1]
Precharge all
Wait until tRP is satisfied
MRS MR3, Opcode A2='1'b
- Redirect all subsequent read and writes to MPR locations

Wait until tMRD and tMOD satisfied.

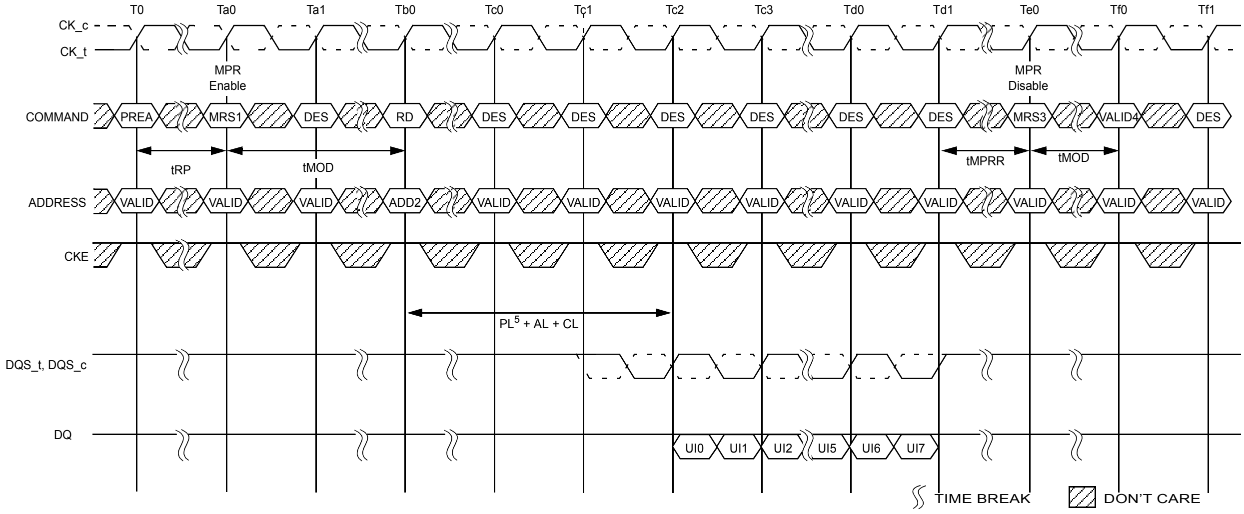
Read command
- A[1:0] = '00'b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= '0'b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
(For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)

or
- A[2]= 1 (For BL=8 : Not Support)
(For BC=4, burst order is fixed at 4,5,6,7,T,T,T,T)
- A12/BC= 0 or 1 : Burst length supports only BL8(Fixed) and BC4(Fixed), not supports BC4(OTF).

When MR0 A[1:0] is set "01" , A12/BC must be always '1'b in MPR read commands (BL8 only).
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG1and BG0

After RL= AL + CL, DRAM bursts out the data from MPR location. The format of data on return is described in a later section and controlled by MR3 bits A0,A1, A11 and A12.
Memory controller repeats these calibration reads until read data capture at memory controller is optimized. Read MPR location can be a different location as specified by the Read command
After end of last MPR read burst, wait until tMPRR is satisfied
MRS MR3, Opcode A2= '0b'
All subsequent reads and writes from DRAM array
Wait until tMRD and tMOD are satisfied
Continue with regular DRAM commands like Activate.

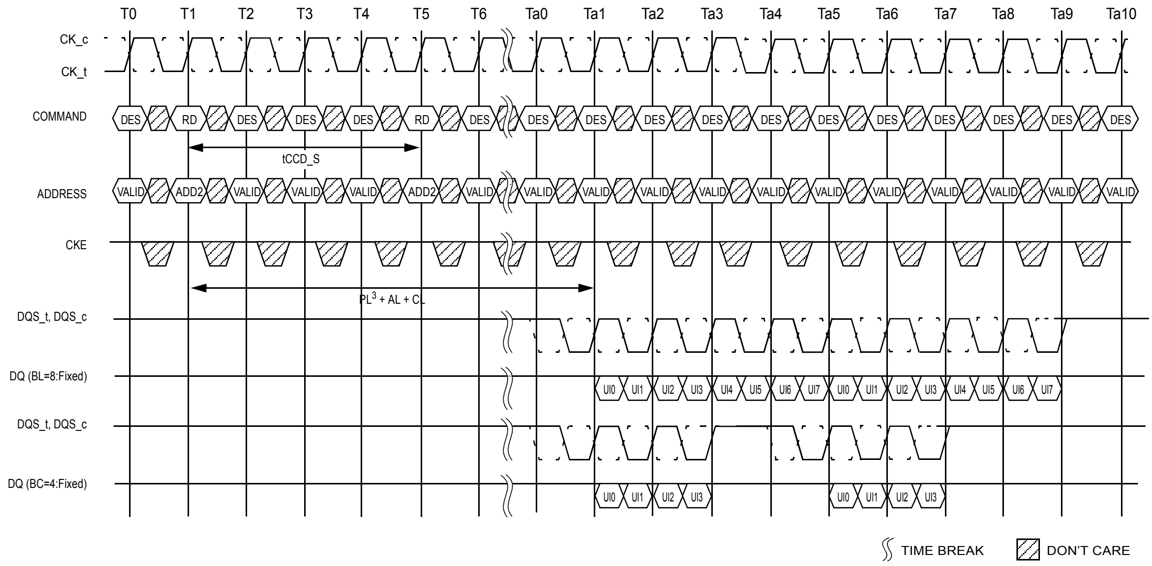
This process is depicted below(PL=0).



NOTE :

1. Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
- Redirect all subsequent read and writes to MPR locations
2. Address setting
- A[1:0] = “00”b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= “0”b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = “00” or “10” , and must be ‘1’b when MR0 A[1:0] = “01”
3. Multi-Purpose Registers Read/Write Disable (MR3 A2 = 0)
4. Continue with regular DRAM command.
5. PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

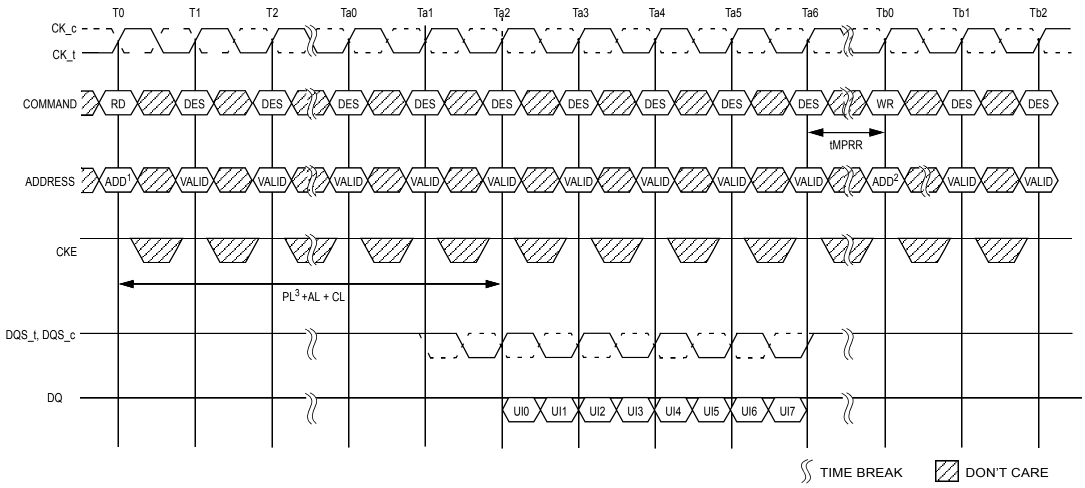
Figure 12. MPR Read Timing



NOTE :

1. tCCD_S = 4, Read Preamble = 1tCK
2. Address setting
- A[1:0] = “00”b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= “0”b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
  (For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = “00” or “10” , and must be ‘1’b when MR0 A[1:0] = “01”
3. PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

Figure 13. MPR Back to Back Read Timing



NOTE :
1. Address setting
- A[1:0] = “00”b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= “0”b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = “00”, and must be ‘1’b when MR0 A[1:0] = “01”
2. Address setting
- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don’t care.
3. PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

Figure 14. MPR Read to Write Timing

2.10.4 MPR Writes

DDR4 allows 8 bit writes to the MPR location using the address bus A7:A0.

[Table 32] UI and Address Mapping for MPR Location

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SDRAM Address	A7	A6	A5	A4	A3	A2	A1	A0
UI	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

STEPS:
DLL must be locked prior to MPR Writes. If DLL is Enabled : MR1[A0 = 1]
Precharge all
Wait until tRP is satisfied
MRS MR3, Opcode A2=’1’b
Redirect all subsequent read and writes to MPR locations

Wait until tMRD and tMOD satisfied.

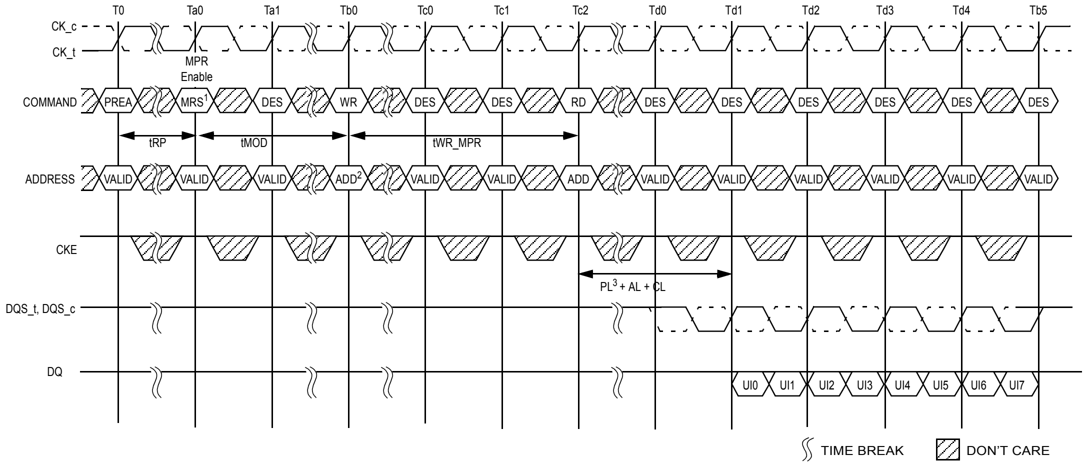
Write command
BA1 and BA0 indicate the MPR location
A [7:0] = data for MPR

Wait until tWR_MPR satisfied, so that DRAM to complete MPR write transaction.

Memory controller repeats these calibration writes and reads until data capture at memory controller is optimized.
After end of last MPR read burst, wait until tMPRR is satisfied
MRS MR3, Opcode A2= ‘0b’
All subsequent reads and writes from DRAM array

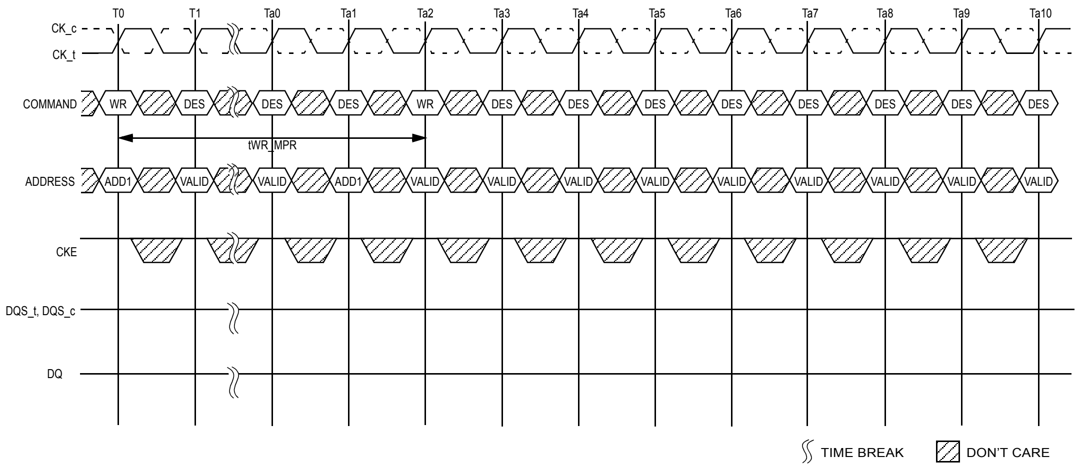
Wait until tMRD and tMOD are satisfied
Continue with regular DRAM commands like Activate.

This process is depicted in Figure 15.



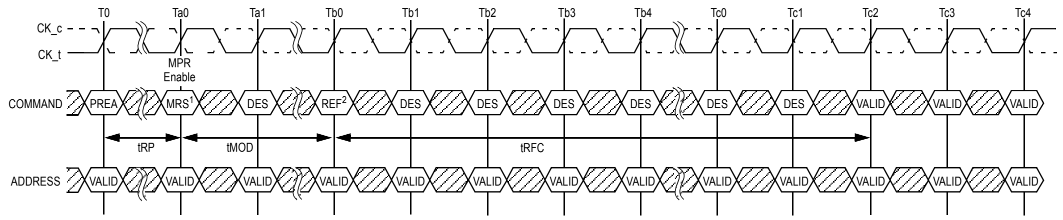
NOTE :
1. Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
2. Address setting - BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.
3. PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

Figure 15. MPR Write Timing and Write to Read Timing



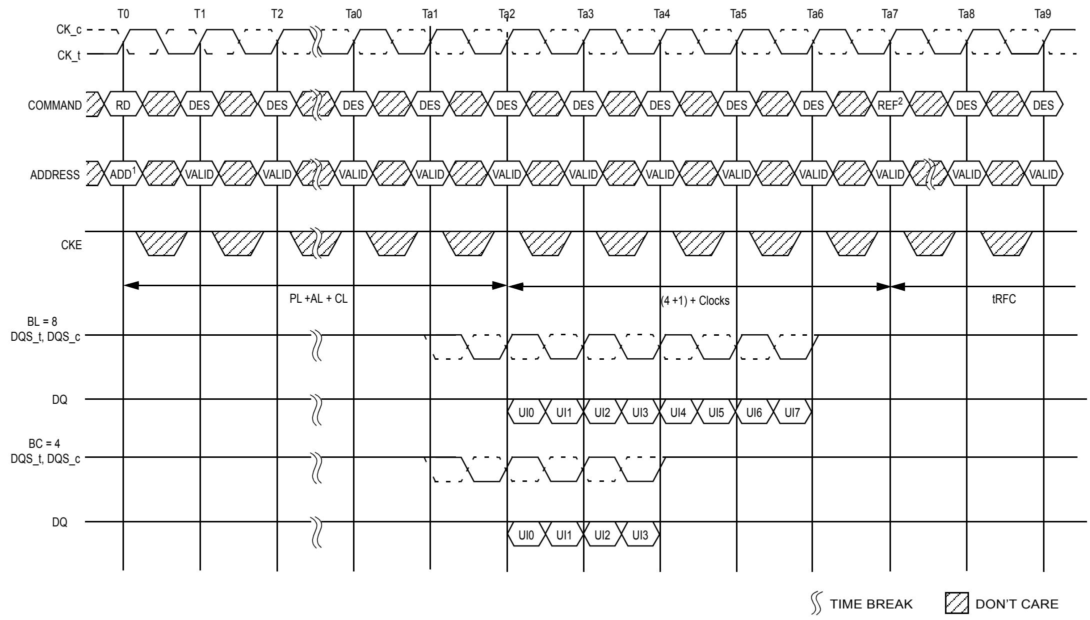
NOTE :
1. Address setting
- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

Figure 16. MPR Back to Back Write Timing



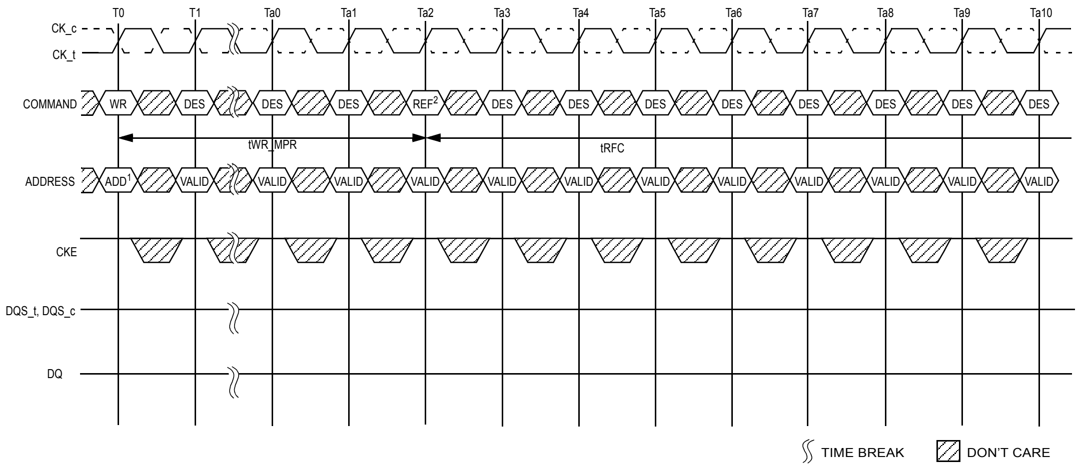
NOTE :
1.Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
- Redirect all subsequent read and writes to MPR locations
2. 1x Refresh is only allowed when MPR mode is Enable.

Figure 17. Refresh Command Timing



NOTE :
1. Address setting
- A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG1 and BG0. A12 is don't care when MR0 A[1:0] = "00" or "10" , and must be '1'b when MR0 A[1:0] = "01"
2. 1x Refresh is only allowed when MPR mode is Enable.

Figure 18. Read to Refresh Command Timing



NOTE
1. Address setting - BA1 and BA0 indicate the MPR location - A [7:0] = data for MPR
   - A10 and other address pins are don't care.
2. 1x Refresh is only allowed when MPR mode is Enable.

Figure 19. Write to Refresh Command Timing

2.10.5 MPR Read Data format

Mode bits in MR3: (A12, A11) are used to select the data return format for MPR reads. The DRAM is required to drive associated strobes with the read data returned for all read data formats.

Serial return implies that the same pattern is returned on all DQ lanes as shown in figure below. Data from the MPR is used on all DQ lanes for the serial return case. Reads from MPR page0, MPR page1,MPR page2 and MPR page3 are alllowed with serial data return mode.
In this example the pattern programmed in the MPR register is 0111 1111 in MPR Location [7:0].

x4 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1

x8 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

x16 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

Parallel return implies that the MPR data is retuned in the first UI and then repeated in the remaining UI's of the burst as shown in the figure below. Data from Page0 MPR registers can be used for the parallel return case as well. Read from MPR page1, MPR page2 and MPR page3 are not allowed with parallel data return mode. In this example the pattern programmed in the Page 0 MPR register is 0111 1111:MPR Location [7:0] . For the case of x4, only the first four bits are used (0111:MPR Location [7:4] in this example). For the case of x16, the same pattern is repeated on upper and lower bytes.

x4 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1

x8 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1

x16 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

The third mode of data return is the staggering of the MPR data across the lanes. In this mode a read command is issued to a specific MPR and then the data is returned on the DQ from different MPR registers. Read from MPR page1, MPR page2, and MPR page3 are not allowed with staggered data return mode.

For a x4 device, a read to MPR0 will result in data from MPR0 being driven on DQ0, data from MPR1 on DQ1 and so forth as shown below.

A read command to MPR1 will result in data from MPR1 being driven on DQ0, data from MPR2 on DQ1 and so forth as shown below.
Reads from MPR2 and MPR3 are also shown below.

x4 (Read MPR0 command)

Stagger	UI0-7
DQ0	MPR0
DQ1	MPR1
DQ2	MPR2
DQ3	MPR3

x4 (Read MPR1 command)

Stagger	UI0-7
DQ0	MPR1
DQ1	MPR2
DQ2	MPR3
DQ3	MPR0

x4 (Read MPR2 command)

Stagger	UI0-7
DQ0	MPR2
DQ1	MPR3
DQ2	MPR0
DQ3	MPR1

x4 (Read MPR3 command)

Stagger	UI0-7
DQ0	MPR3
DQ1	MPR0
DQ2	MPR1
DQ3	MPR2

It is expected that the DRAM can respond to back to back read commands to MPR for all DDR4 frequencies so that a stream as follows can be created on the data bus with no bubbles or clocks between read data. In this case controller issues a sequence of RD MPR0, RD MPR1, RD MPR2, RD MPR3, RD MPR0, RD MPR1, RD MPR2 and RD MPR3.

x4 (Back to Back read commands)

Stagger	UI 0-7	UI 8-15	UI 16-23	UI 24-31	UI 32-39	UI 40-47	UI 48-55	UI 56-63
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

The following figure shows a read command to MPR0 for a x8 device. The same pattern is repeated on the lower nibble as on the upper nibble. Reads to other MPR location follows the same format as for x4 case.

A read example to MPR0 for x8 and x16 device is shown below.

x8 (Read MPR0 command)

Stagger	UI0-7
DQ0	MPR0
DQ1	MPR1
DQ2	MPR2
DQ3	MPR3
DQ4	MPR0
DQ5	MPR1
DQ6	MPR2
DQ7	MPR3

x16 (Read MPR0 command)

Stagger	UI0-7
DQ0	MPR0
DQ1	MPR1
DQ2	MPR2
DQ3	MPR3
DQ4	MPR0
DQ5	MPR1
DQ6	MPR2
DQ7	MPR3
DQ8	MPR0
DQ9	MPR1
DQ10	MPR2
DQ11	MPR3
DQ12	MPR0
DQ13	MPR1
DQ14	MPR2
DQ15	MPR3

DDR4 MPR mode enable and page selection is done by Mode Register command as shown below.

[Table 33] MPR MR3 Register Definition

Address	Operating Mode	Description
A2	MPR operaion	0 = Normal 1 = Dataflow from/to MPR
A1:A0	MPR selection	00 = page0 01 = page1 10 = page2 11 = page3
A12:A11	MPR Read Format	00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved

Four MPR pages are provided in DDR4 SDRAM. Page 0 is for both read and write, and pages 1,2 and 3 are read-only. Any MPR location (MPR0-3) in page 0 can be readable through any of three readout modes (serial, parallel or staggered), but pages 1, 2 and 3 support only the serial readout mode.

After power up, the content of MPR page 0 should have the default value as defined in the table. MPR page 0 can be writeable only when MPR write command is issued by controller. Unless MPR write command is issued, DRAM must keep the default value permanently, and should never change the content on its own for any purpose. When MPR write command is issued to any of read-only pages (page 1, 2 or 3), the command is ignored by DRAM.

[Table 34] MPR data format

MPR page0 (Training pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01= MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

NOTE :
1. MPRx using A7:A0 that A7 is mapped to location [7] and A0 is mapped to location [0].

MPR page1 (CA parity error log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-only
	01 = MPR1	CAS_n/ A15	WE_n/ A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	ACT_n	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	RAS_n/ A16	
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency[4]			C[2]	C[1]	C[0]	
				MR5.A[2]	MR5.A[1]	MR5.A[0]				

NOTE :
1. MPR used for C/A parity error log readout is enabled by setting A[2] in MR3
2. For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.
3. If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

MPR page2 (MRS Readout)

<table>
<tr><th>Address</th><th>MPR Location</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>note</th></tr>
<tr><td rowspan="12">BA1:BA0</td><td rowspan="3">00 = MPR0</td><td>PPR</td><td>RFU</td><td>RTT_WR</td><td colspan="2">Temperature Sensor Status</td><td>CRC Write Enable</td><td colspan="2">Rtt_WR</td><td rowspan="12">read-only</td></tr>
<tr><td>-</td><td>-</td><td>MR2</td><td>-</td><td>-</td><td>MR2</td><td colspan="2">MR2</td></tr>
<tr><td>-</td><td>-</td><td>A11</td><td>-</td><td>-</td><td>A12</td><td>A10</td><td>A9</td></tr>
<tr><td rowspan="3">01= MPR1</td><td>Vref DQ Trng range</td><td colspan="6">Vref DQ training Value</td><td>Gear-down Enable</td></tr>
<tr><td>MR6</td><td colspan="6">MR6</td><td>MR3</td></tr>
<tr><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>A3</td></tr>
<tr><td rowspan="3">10 = MPR2</td><td colspan="4">CAS Latency</td><td>RFU</td><td colspan="3">CAS Write Latency</td></tr>
<tr><td colspan="4">MR0</td><td>-</td><td colspan="3">MR2</td></tr>
<tr><td>A6</td><td>A5</td><td>A4</td><td>A2</td><td>-</td><td>A5</td><td>A4</td><td>A3</td></tr>
<tr><td rowspan="3">11 = MPR3</td><td colspan="3">Rtt_Nom</td><td colspan="3">Rtt_Park</td><td colspan="2">Driver Impedance</td></tr>
<tr><td colspan="3">MR1</td><td colspan="3">MR5</td><td colspan="2">MR1</td></tr>
<tr><td>A10</td><td>A9</td><td>A8</td><td>A8</td><td>A7</td><td>A6</td><td>A2</td><td>A1</td></tr>
</table>

MPR page3 (MPR0 through MPR2 in MPR page3 are for Vendor use only)

<table>
<tr><th>Address</th><th>MPR Location</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>note</th></tr>
<tr><td rowspan="4">BA1:BA0</td><td>00 = MPR0</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td rowspan="4">read-only</td></tr>
<tr><td>01= MPR1</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td></tr>
<tr><td>10 = MPR2</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td></tr>
<tr><td>11 = MPR3</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>don’t care</td><td>MAC</td><td>MAC</td><td>MAC</td><td>MAC</td></tr>
</table>

[Table 35] DDR4 MPR Page3 MAC Decode Value

MPR Location	A7:A4	A2	A1	A0	Note
Reserved	X	1	1	1	2
Reserved	X	1	1	0	2
MAC>300K	X	1	0	1	
MAC>400K	X	1	0	0	
MAC>500K	X	0	1	1	
MAC>600K	X	0	1	0	
MAC>700K	X	0	0	1	
Unknown	X	0	0	0	1

1. Unknown means that device is not tested for MAC and pass/fail value is unknown
2. Reserved for future device.

[Table 36] Unlimited MAC

	A3	Note
Unlimited MAC	1	1,2

1. Unlimited MAC means that there is no restriction to the number of Activates in a refresh period provided DDR4 specifications are not violated, in particular tRCmin and refresh requirements
2. All other bits A2:A0 are set to zero

2.11 Data Mask(DM), Data Bus Inversion (DBI) and TDQS

DDR4 SDRAM supports Data Mask (DM) function and Data Bus Inversion (DBI) functionon in x8 and x16 DRAM configuration. x4 DDR4 SDRAM does not support DM and DBI function. x8 DDR4 SDRAM supports TDQS function. x4 and x16 DDR4 SDRAM does not support TDQS function.

DM, DBI & TDQS functions are supported with dedicated one pin labeled as DM_n/DBI_n/TDQS_t. The pin is bi-directional pin for DRAM. The DM_n/DBI_n pin is Active Low as DDR4 supports VDDQ reference termination. TDQS function does not drive actual level on the pin.

DM, DBI & TDQS functions are programmable through DRAM Mode Register (MR). The MR bit location is bit A11 in MR1 and bit A12:A10 in MR5 .
Write operation: Either DM or DBI function can be enabled but both functions cannot be enabled simultanteously. When both DM and DBI functions are disabled, DRAM turns off its input receiver and does not expect any valid logic level.
Read operation: Only DBI function applies. When DBI function is disabled, DRAM turns off its output driver and does not drive any valid logic level.

TDQS function: When TDQS function is enabled, DM & DBI functions are not supported. When TDQS function is disabled, DM and DBI functions are supported as described below in Table 30. When enabled, the same termination resistance function is applied to the TDQS_t/TDQS_c pins that is applied to DQS_t/DQS_c pins.

[Table 37] TDQS Function Matrix

MR1 bit A11	DM (MR5 bit A10)	Write DBI (MR5 bit A11)	Read DBI (MR5 bit A12)
0 (TDQS Disabled)	Enabled	Disabled	Enabled or Disabled
	Disabled	Enabled	Enabled or Disabled
	Disabled	Disabled	Enabled or Disabled
1 (TDQS Enabled)	Disabled	Disabled	Disabled

[Table 38] DRAM Mode Register MR5

A10	DM Enable
0	Disabled
1	Enabled

[Table 39] DRAM Mode Register MR5

A11	Write DBI Enable	A12	Read DBI Enable
0	Disabled	0	Disabled
1	Enabled	1	Enabled

[Table 40] DRAM Mode Register MR1

A11	TDQS Enable
0	Disabled
1	Enabled

DM function during Write operation: DRAM masks the write data received on the DQ inputs if DM_n was sampled Low on a given byte lane. If DM_n was sampled High on a given byte lane, DRAM does not mask the write data and writes into the DRAM core.

DBI function during Write operation: DRAM inverts write data received on the DQ inputs if DBI_n was sampled Low on a given byte lane. If DBI_n was sampled High on a given byte lane, DRAM leaves the data received on the DQ inputs non-inverted.

DBI function during Read operation: DRAM inverts read data on its DQ outputs and drives DBI_n pin Low when the number of ‘0’ data bits within a given byte lane is greater than 4; otherwise DRAM does not invert the read data and drives DBI_n pin High.

[Table 41] x8 DRAM Write DQ Frame Format

	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
DM_n or DBI_n	DM0 or DBI0	DM1 or DBI1	DM2 or DBI2	DM3 or DBI3	DM4 or DBI4	DM5 or DBI5	DM6 or DBI6	DM7 or DBI7

[Table 42] x8 DRAM Read DQ Frame Format

	Data transfer							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
DBI_n	DBI0	DBI1	DBI2	DBI3	DBI4	DBI5	DBI6	DBI7

[Table 43] x16 DRAM Write DQ Frame Format

	Data transfer							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQL[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
DML_n or DBIL_n	DML0 or DBIL0	DML1 or DBIL1	DML2 or DBIL2	DML3 or DBIL3	DML4 or DBIL4	DML5 or DBIL5	DML6 or DBIL6	DML7 or DBIL7
DQU[7:0]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
DMU_n or DBI-U_n	DMU0 or DBIU0	DMU1 or DBIU1	DMU2 or DBIU2	DMU3 or DBIU3	DMU4 or DBIU4	DMU5 or DBIU5	DMU6 or DBIU6	DMU7 or DBIU7

[Table 44] x16 DRAM Read DQ Frame Format

	Data transfer							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQL[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
DBIL_n	DBIL0	DBIL1	DBIL2	DBIL3	DBIL4	DBIL5	DBIL6	DBIL7
DQU[7:0]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
DBIU_n	DBIU0	DBIU1	DBIU2	DBIU3	DBIU4	DBIU5	DBIU6	DBIU7

2.12 ZQ Calibration Commands

2.12.1 ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron & ODT values. DDR4 SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET are allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 128 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

Where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / oC, VSens = 0.15% / mV, Tdriftrate = 1 oC / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

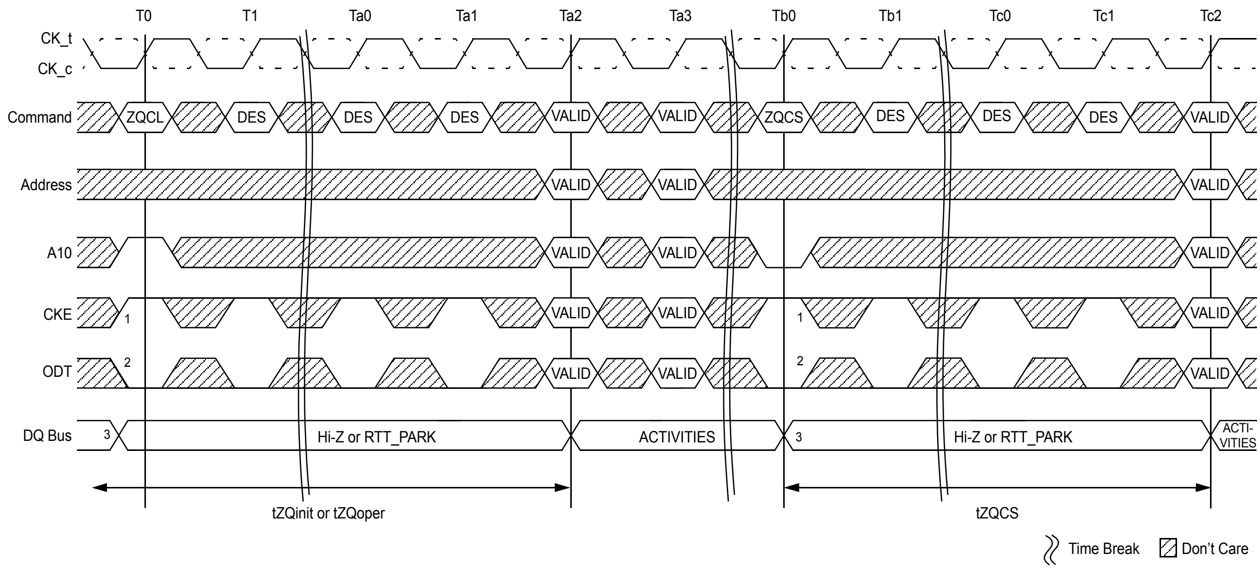
$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\mathit{ms}$$

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller. See "Command Truth Table" on Section 2.1 for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, DDR4 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is XS, XS_Abort/ XS_FAST depending on operation mode.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between the devices.



NOTE :
1. CKE must be continuously registered high during the calibration procedure.
2. During ZQ Calibration, ODT signal must be held LOW and DRAM continues to provide RTT_PARK.
3. All devices connected to the DQ bus should be high impedance or RTT_PARK during the calibration procedure.

Figure 20. ZQ Calibration Timing

2.13 DQ Vref Training

The DRAM internal DQ Vref specification parameters are operating voltage range, stepsize, Vref step time, Vref full step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for DDR4 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in Figure 21 below.

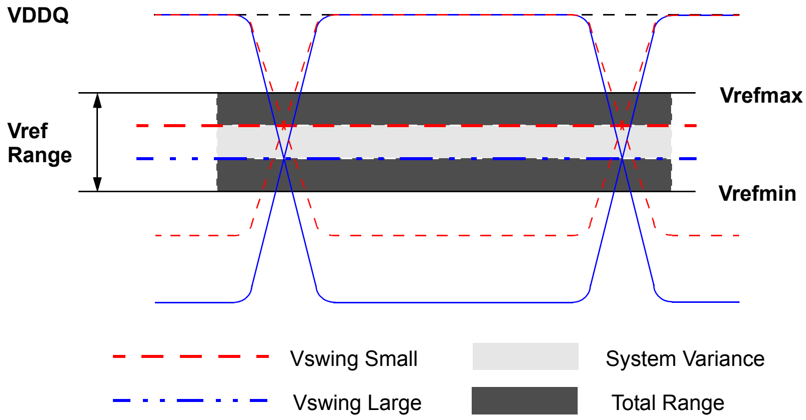


Figure 21. Vref operating range(Vrefmin, Vrefmax)

The Vref stepsize is defined as the stepsize between adjacent steps. Vref stepsize ranges from 0.5% VDDQ to 0.8% VDDQ. However, for a given design, DRAM has one value for Vref step size that falls within the range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainity. The range of Vref set tolerance uncertainty is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

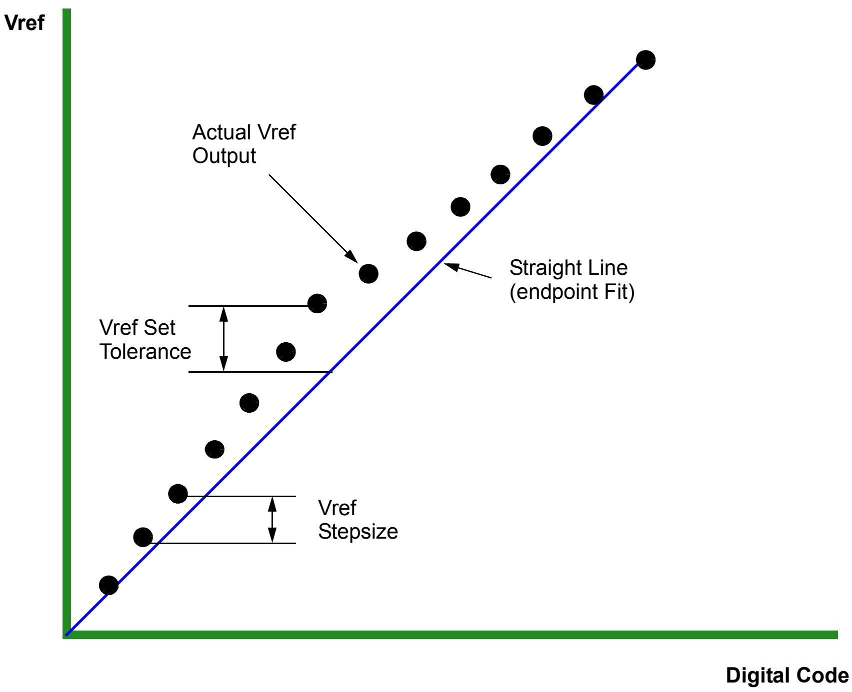


Figure 22. Example of Vref set tolerance(max case only shown) and stepsize

The Vref increment/decrement step times are define by Vref_time. The Vref_time is defined from t0 to t1 as shown in the Figure 23 below where t1 is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance (Vref_val_tol).

The Vref valid level is defined by Vref_val tolerance to qualify the step time t1 as shown in Figure 25 through Figure 28. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

Vref_time is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change in Vref voltage.

t0 - is referenced to MRS command clock
t1 - is referenced to the Vref_val_tol

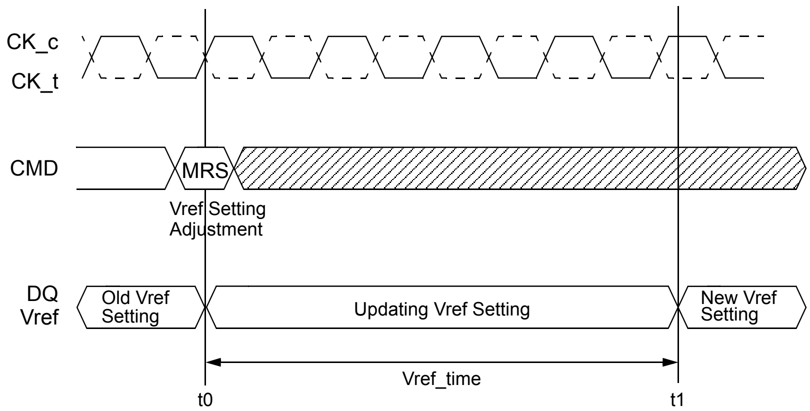
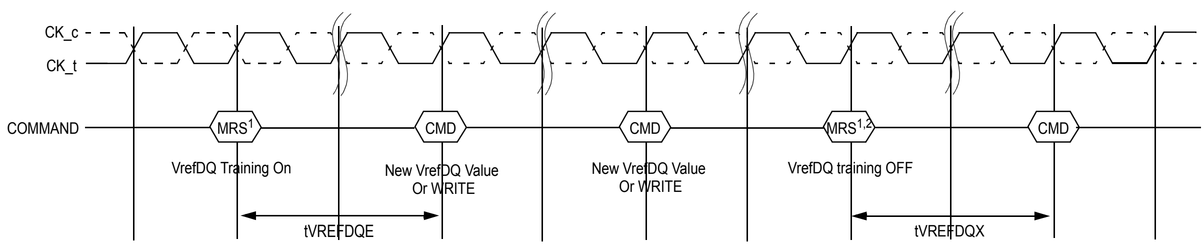


Figure 23. Vref_time timing diagram

VrefDQ Calibration Mode is entered via MRS command setting MR6 A[7] to 1 (0 disables VrefDQ Calibration Mode), setting MR6 A[6] to either 0 or 1 to select the desired range, and MR6 A[5:0] with a “don’t care” setting (there is no default initial setting; whether VrefDQ training value (MR6 A[5:0]) at training mode entry with MR6 A[7]=1 is captured by the DRAM or not is vendor specific). The next subsequent MR command is used to set the desired VrefDQ values at MR6 A[5:0]. Once VrefDQ Calibration Mode has been entered, VrefDQ Calibration Mode legal commands may be issued once tVREFDQE has been satisfied. VrefDQ Calibration Mode legal commands are ACT, WR, WRA, RD, RDA, PRE, DES, MRS to set VrefDQ values, and MRS to exit VrefDQ Calibration Mode. Once VrefDQ Calibration Mode has been entered, “dummy” write commands may be issued prior to adjusting VrefDQ value the first time VrefDQ calibration is performed after initialization. The “dummy” write commands may have bubbles bewtween write commands provided other DRAM timings are satisfied. A possible example command sequence would be: WR1, DES, DES, DES, WR2, DES, DES, DES, WR3, DES, DES, DES, WR4, DES, DES…….DES, DES, WR50, DES, DES, DES. Setting VrefDQ values requires MR6 [7] set to 1, MR6 [6] unchanged from initial range selection, and MR6 A[5:0] set to desired VrefDQ value; if MR6 [7] is set to 0, MR6 [6;0] are not written. Vref_time must be satisfied after each MR6 command to set VrefDQ value before the internal VrefDQ value is valid.

If PDA mode is used in conjunction with VrefDQ calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only VrefDQ Calibration Mode legal commands noted above that may be used are the MRS commands, i.e. MRS to set VrefDQ values, and MRS to exit VrefDQ Calibration Mode.

The last A[6:0] setting written to MR6 prior to exiting VrefDQ Calibration Mode is the range and value used for the internal VrefDQ setting. VrefDQ Calibration Mode may be exited when the DRAM is in idle state. After the MRS command to exit VrefDQ Calibration Mode has been issued, DES must be issued till tVREFDQX has been satisfied where any legal command may then be issued.



NOTE :

1. The MR command used to enter VrefDQ Calibration Mode treats MR6 A[5:0] as don’t care while the next subsequent MR command sets VrefDQ values in MR6 A[5:0] .
2. Depending on the step size of the latest programmed VREF value, Vref_time must be satisfied before disabling VrefDQ training mode.

Figure 24. VrefDQ training mode entry and exit timing diagram

[Table 45] AC parameters of DDR4 VrefDQ training

Speed		DDR4-1600,1866,2133,2400,2666,3200		Units	NOTE
Parameter	Symbol	MIN	MAX		
VrefDQ training					
Enter VrefDQ training mode to the first valid command delay	tVREFDQE	150	-	ns	
Exit VrefDQ training mode to the first valid command delay	tVREFDQX	150	-	ns	

2.13.1 Example scripts for VREFDQ Calibration Mode:

When MR6 [7] = 0 then MR6 [6:0] = XXXXXXX

Entering VREFDQ Calibration if entering range 1:
- MR6 [7:6]=10 & [5:0]=XXXXXX
- All subsequent VREFDQ Calibration MR setting commands are MR6 [7:6]=10 & MR6 [5:0]=VVVVVV
  {VVVVVV are desired settings for VrefDQ}
- Issue ACT/WR/RD looking for pass/fail to determine Vcent(midpoint) as needed
- Just prior to exiting VREFDQ Calibration mode:
- Last two VREFDQ Calibration MR commands are
- MR6 [7:6]=10, MR6 [5:0]=VVVVVV’ where VVVVVV’ = desired value for VREFDQ
- MR6 [7]=0, MR6 [6:0]=XXXXXXX to exit VREFDQ Calibration mode

Entering VREFDQ Calibration if entering range 2:
- MR6 [7:6]=11 & [5:0]=XXXXXX
- All subsequent VREFDQ Calibration MR setting commands are MR6 [7:6]=11 & MR6 [5:0]=VVVVVV
  {VVVVVV are desired settings for VrefDQ}
- Issue ACT/WR/RD looking for pass/fail to determine Vcent(midpoint) as needed
- Just prior to exiting VREFDQ Calibration mode:
- Last two VREFDQ Calibration MR commands are
- MR6 [7:6]=11, MR6 [5:0]=VVVVVV’ where VVVVVV’ = desired value for VREFDQ
- MR6 [7]=0, MR6 [6:0]=XXXXXXX to exit VREFDQ Calibration mode

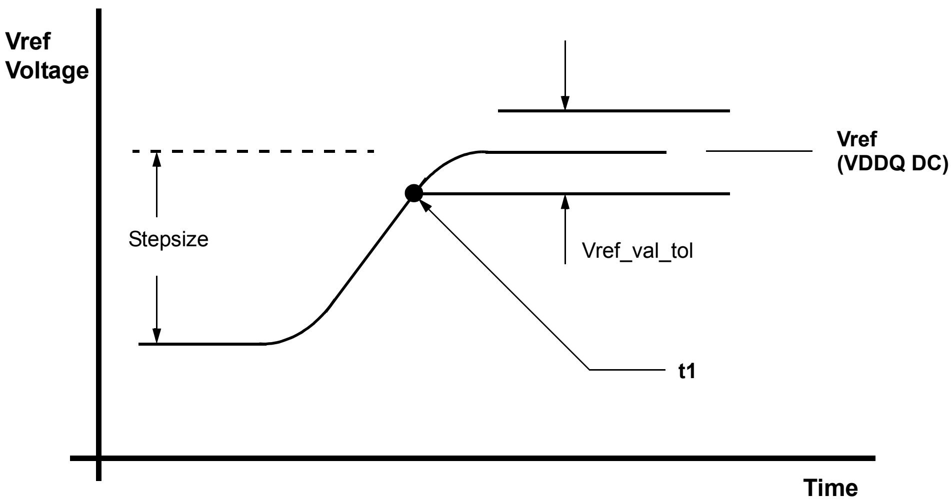


Figure 25. Vref step single stepsize increment case

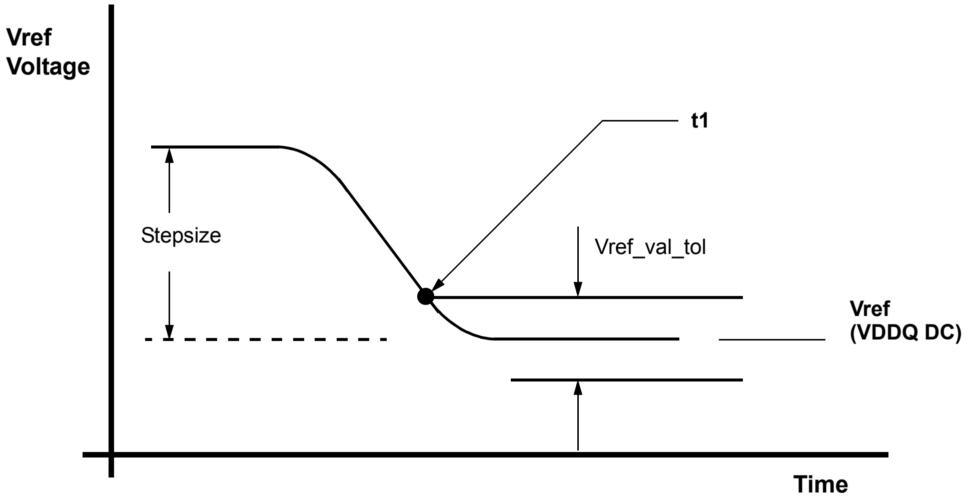


Figure 26. Vref step single stepsize decrement case

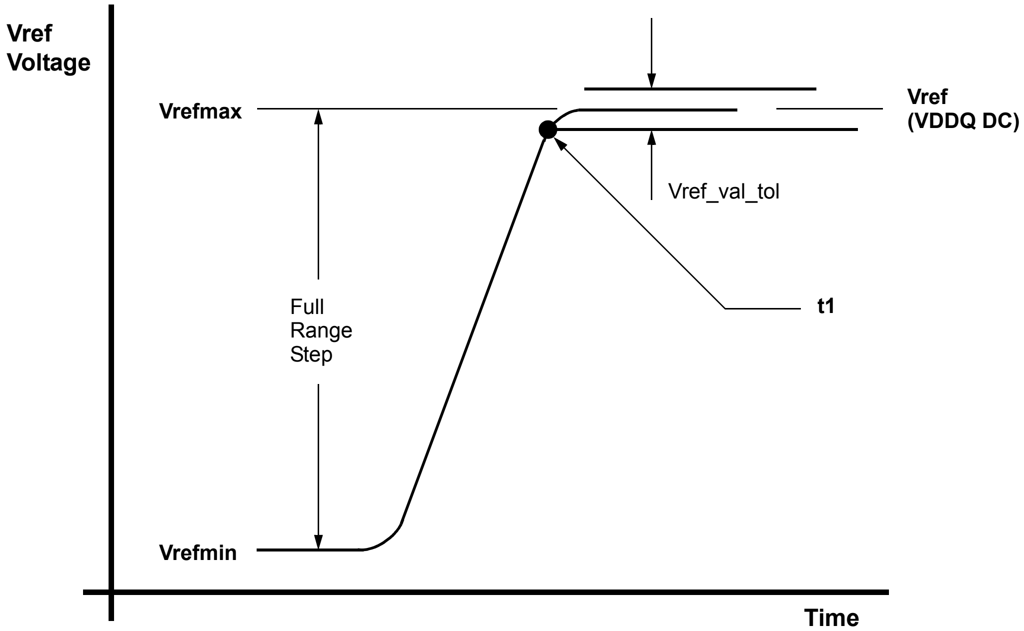


Figure 27. Vref full step from Vrefmin to Vrefmax case

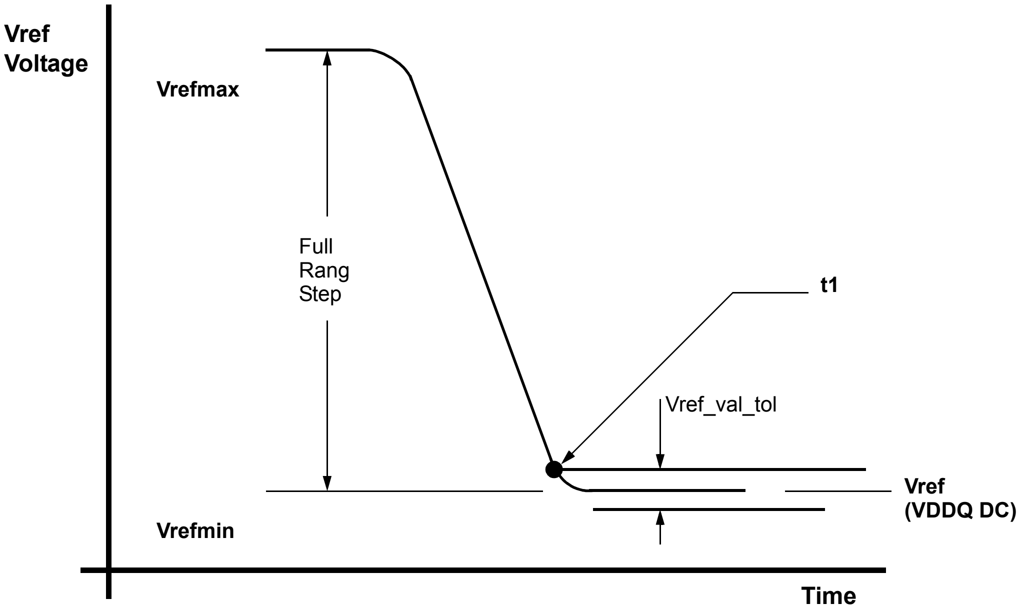


Figure 28. Vref full step from Vrefmax to Vrefmin case

[Table 46] DQ Internal Vref Specifications

Prarmeter	Symbol	Min	Typ	Max	Unit	NOTE
Vref Max operating point Range1	$V_{ref\_max\_R1}$	92%	-	-	VDDQ	1, 10
Vref Min operating point Range1	$V_{ref\_min\_R1}$	-	-	60%	VDDQ	1, 10
Vref Max operating point Range2	$V_{ref\_max\_R2}$	77%	-	-	VDDQ	1, 10
Vref Min operating point Range2	$V_{ref\_min\_R2}$	-	-	45%	VDDQ	1, 10
Vref Stepsize	$V_{ref\ step}$	0.50%	0.65%	0.80%	VDDQ	2
Vref Set Tolerance	$V_{ref\_set\_tol}$	-1.625%	0.00%	1.625%	VDDQ	3,4,6
		-0.15%	0.00%	0.15%	VDDQ	3,5,7
Vref Step Time	V_{ref_time}	-	-	150	ns	8,11
Vref Valid tolerance	$V_{ref\_val\_tol}$	-0.15%	0.00%	0.15%	VDDQ	9

NOTE :
1. Vref DC voltage referenced to VDDQ_DC. VDDQ_DC is 1.2V
2. Vref stepsize increment/decrement range. Vref at DC level.
3. Vref_new = Vref_old+n*Vref_step; n=number of step; if increment use "+"; If decrement use "-"
4. The minimum value of Vref setting tolerance=Vref_new-1.625%*VDDQ. The maximum value of Vref setting tolerance=Vref_new+1.625%*VDDQ. for n>4
5. The minimum value of Vref setting tolerance=Vref_new-0.15%*VDDQ. The maximum value of Vref setting tolerance=Vref_new+0.15%*VDDQ. for n>4
6. Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line
7. Measured by recording the min and max values of the Vref output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line
8. Time from MRS command to increment or decrement one step size up to full range of Vref
9. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
10. DRAM range1 or 2 set by MRS bit MR6,A6.
11.If the Vref monitor is enabled, Vref_time must be derated by: +10ns if DQ load is 0pF and an additional +15ns/pF of DQ loading.

2.14 Per DRAM Addressability

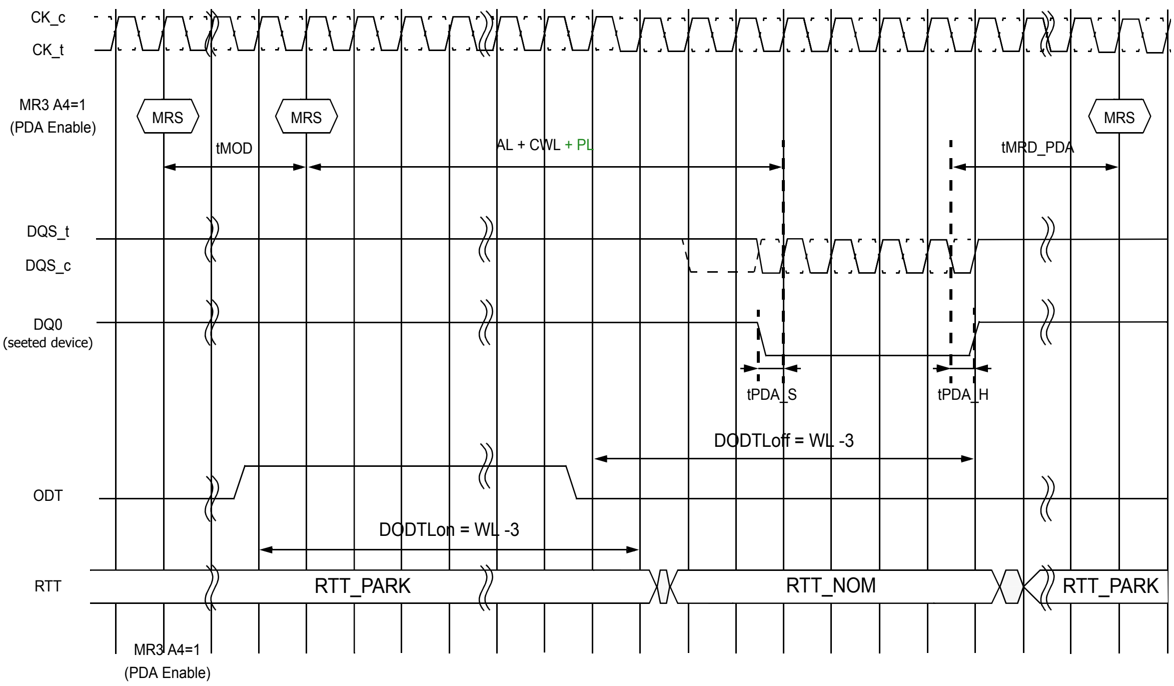
DDR4 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or Vref values on DRAM devices on a given rank.

1. Before entering 'per DRAM addressability (PDA)' mode, the write leveling is required.
2. Before entering 'per DRAM addressability (PDA)' mode, the following Mode Register setting is possible.
   -RTT_PARK MR5 {A8:A6} = Enable
   -RTT_NOM MR1 {A10:A9:A8} = Enable
3. Enable 'per DRAM addressability (PDA)' mode using MR3 bit "A4=1".
4. In the 'per DRAM addressability' mode, all MRS command is qualified with DQ0 for x4 and x8, and DQL0 for x16. DRAM captures DQ0 for x4 and x8, and DQL0 for x16 by using DQS_c and DQS_t for x4 and x8, DQSL_c and DQSL_t for x16 signals as shown Figure 29 . If the value on DQ0 for x4 and x8, and DQL0 for x16 is 0 then the DRAM executes the MRS command. If the value on DQ0 is 1, then the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
5. Program the desired devices and mode registers using MRS command and DQ0 for x4 and x8, and DQL0 for x16.
6. In the 'per DRAM addressability' mode, only MRS commands are allowed.
7. The mode register set command cycle time at PDA mode, AL + CWL + BL/2 - 0.5tCK+ tMRD_PDA + (PL) is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 29.
8. Remove the DRAM from 'per DRAM addressability' mode by setting MR3 bit "A4=0". (This command will require DQ0=0 for x4 andx8, and DQL0 for x16 which shown in Figure 30.

Note:
Removing a DRAM from per DRAM addressability mode will require programming the entire MR3 when the MRS command is issued. This may impact some per DRAM values programmed within a rank as the exit command is sent to the rank. In order to avoid such a case the PDA Enable/Disable Control bit is located in a mode register that does not have any 'per DRAM addressability' mode controls. In per DRAM addressability mode, DRAM captures DQ0 for x4 and x8, and DQL0 for x16 using DQS_t and DQS_c for x4 and x8, DQSL_c and DQSL_t for x16like normal write operation. However, Dynamic ODT is not supported. So extra care required for the ODT setting. If RTT_NOM MR1 {A10:A9:A8} = Enable, DDR4 SDRAM data termination need to be controlled by ODT pin and apply the same timing parameters as defined in Direct ODT function that shown in Table 40. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.

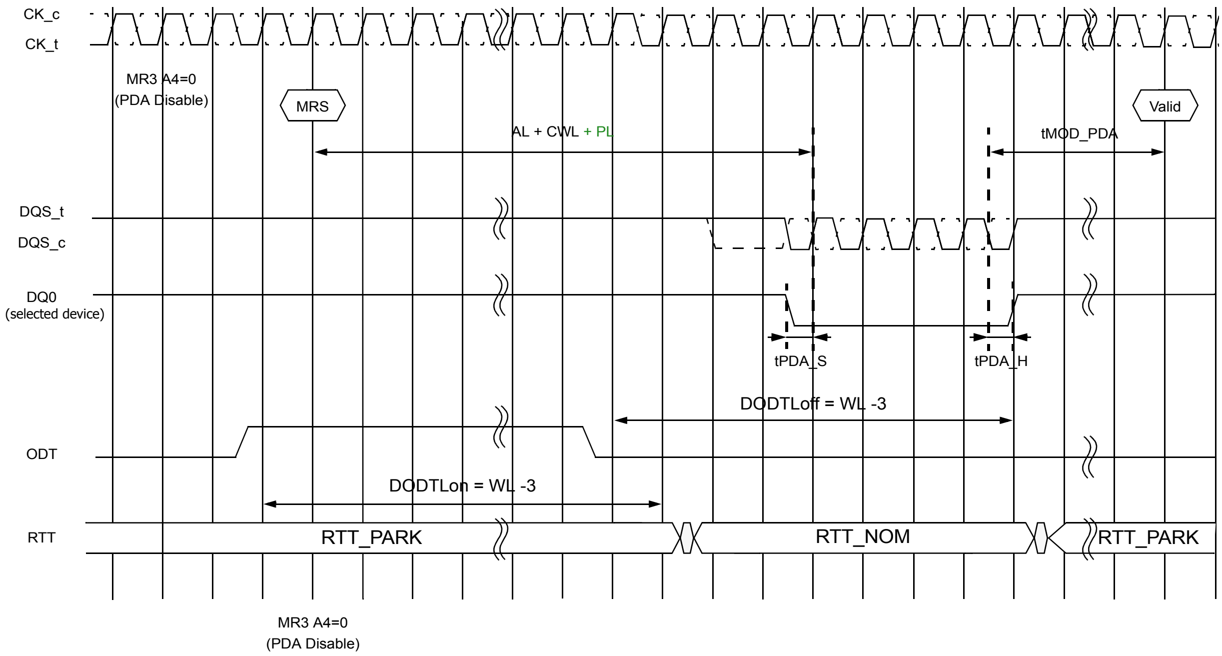
[Table 47] Applied ODT Timing Parameter to PDA Mode

Symbol	Parameter
DODTLon	Direct ODT turn on latency
DODTLoff	Direct ODT turn off latency
tADC	RTT change timing skew
tAONAS	Asynchronous RTT_NOM turn-on delay
tAOFAS	Asynchronous RTT_NOM turn-off delay



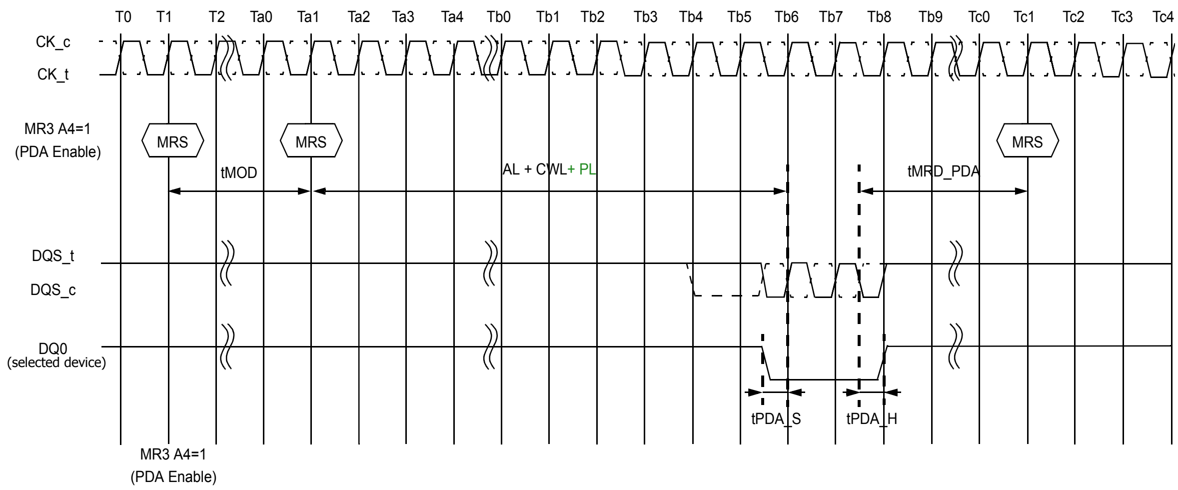
NOTE : RTT_PARK = Enable, RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON, CA parity is used

Figure 29. MRS w/ per DRAM addressability (PDA) issuing before MRS



NOTE : RTT_PARK = Enable, RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON, CA parity is used

Figure 30. MRS w/ per DRAM addressability (PDA) Exit



NOTE : CA parity is used

Figure 31. PDA using Burst Chop 4

Since PDA mode may be used to program optimal Vref for the DRAM, the DRAM may incorrectly read DQ level at the first DQS edge and the last falling DQS edge. It is recommended that DRAM samples DQ0 or DQL0 on either the first falling or second rising DQS edges. This will enable a common implementation between BC4 and BL8 modes on the DRAM. Controller is required to drive DQ0 or DQL0 to a 'Stable Low or High' during the length of the data transfer for BC4 and BL8 cases.

2.15 CAL Mode (CS_n to Command Address Latency)

2.15.1 CAL Mode Description

DDR4 supports Command Address Latency, CAL, function as a power savings feature. CAL is the delay in clock cycles between CS_n and CMD/ADDR defined by MR4[A8:A6] (See Figure 32).
CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched,the receivers can be disabled. For consecutive commands, the DRAM will keep the receivers enabled for the duration of the command sequence (See Figure 33)

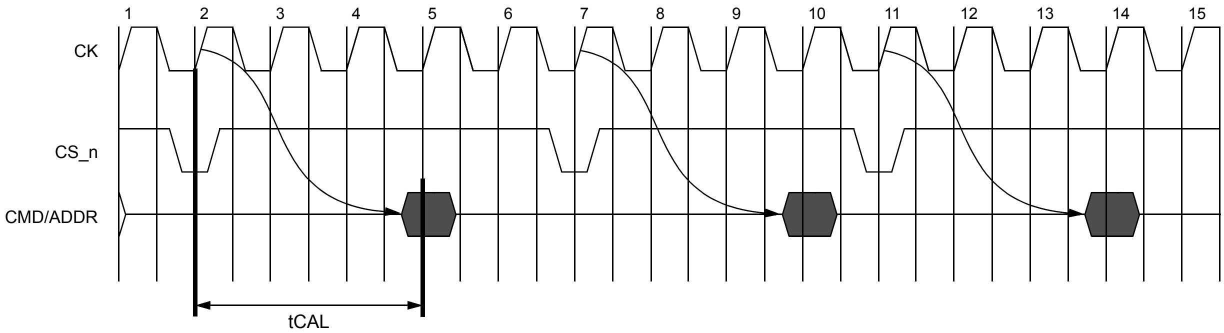


Figure 32. Definition of CAL

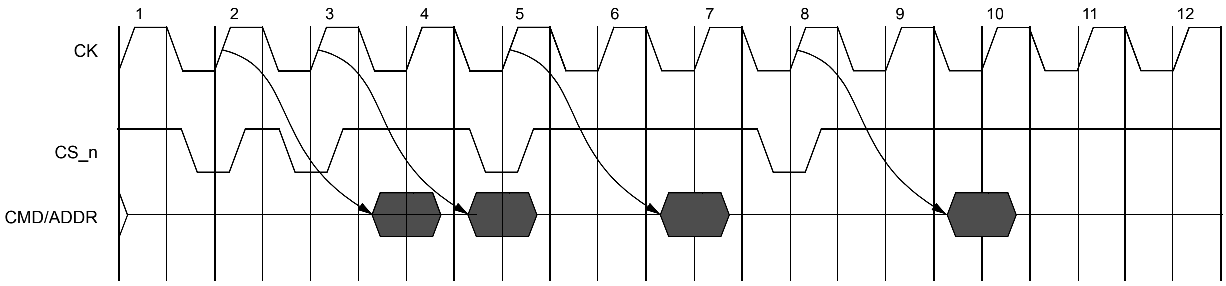


Figure 33. CAL operational timing for consecutive command issues

The following tables show the timing requirements for tCAL (Table 41) and MRS settings (Table 42) at different data rates.

[Table 48] CS to Command Address Latency

Parameter	Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Units
CS to Command Address Latency	CAL	3	4	4	5	nCK

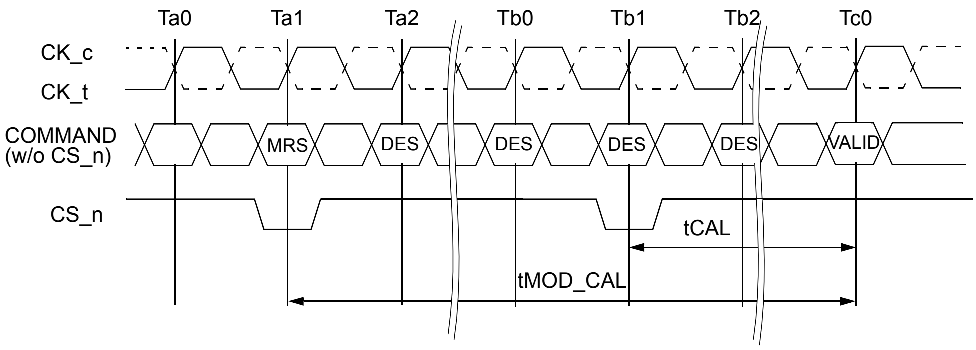
Parameter	Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Units
CS to Command Address Latency (Gear down mode even CK)	CAL	4	4	4	6	nCK

[Table 49] MRS settings for CAL

A8:A6 @ MR4	CAL(tCK cycles)
000	default(disable)
001	3
010	4
011	5
100	6
101	8
110	Reserve
111	Reserve

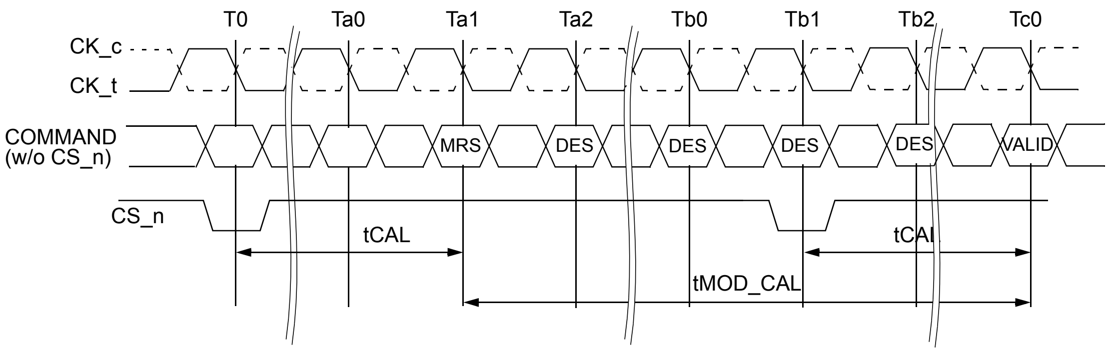
MRS Timings with Command/Address Latency enabled

When Command/Address latency mode is enabled, users must allow more time for MRS commands to take effect. When CAL mode is enabled, or being enabled by an MRS command, the earliest the next valid command can be issued is tMOD_CAL, where tMOD_CAL=tMOD+tCAL.



NOTE :
1. MRS command at Ta1 enables CAL mode
2. tMOD_CAL=tMOD+tCAL

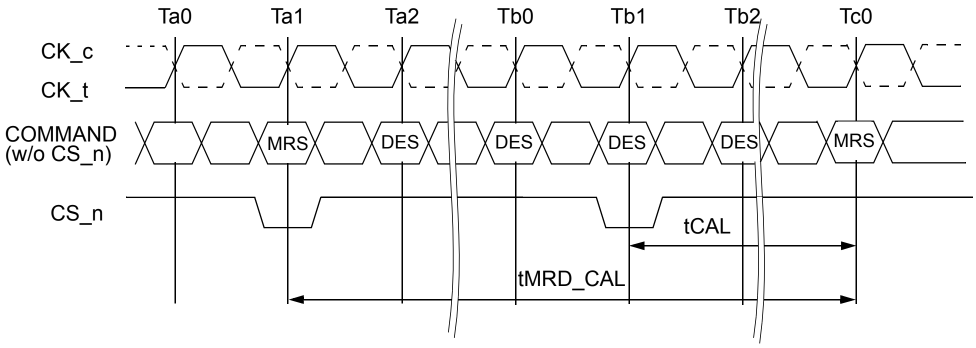
Figure 34. CAL enable timing - tMOD_CAL



NOTE :
1. MRS at Ta1 may or may not modify CAL, tMOD_CAL is computed based on new tCAL setting.
2. tMOD_CAL=tMOD+tCAL.

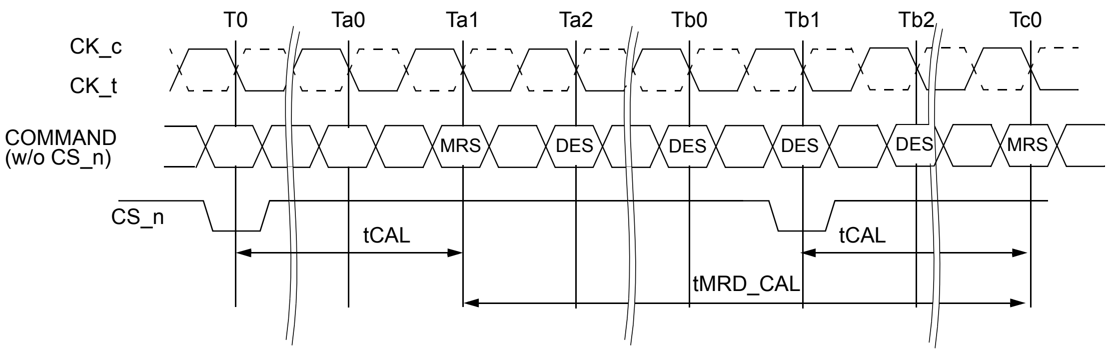
Figure 35. tMOD_CAL, MRS to valid command timing with CAL enabled

When Command/Address latency is enabled or being entered, users must wait tMRD_CAL until the next MRS command can be issued. tMRD_-CAL=tMOD+tCAL.



NOTE :
1. MRS command at Ta1 enables CAL mode
2. tMRD_CAL=tMOD+tCAL

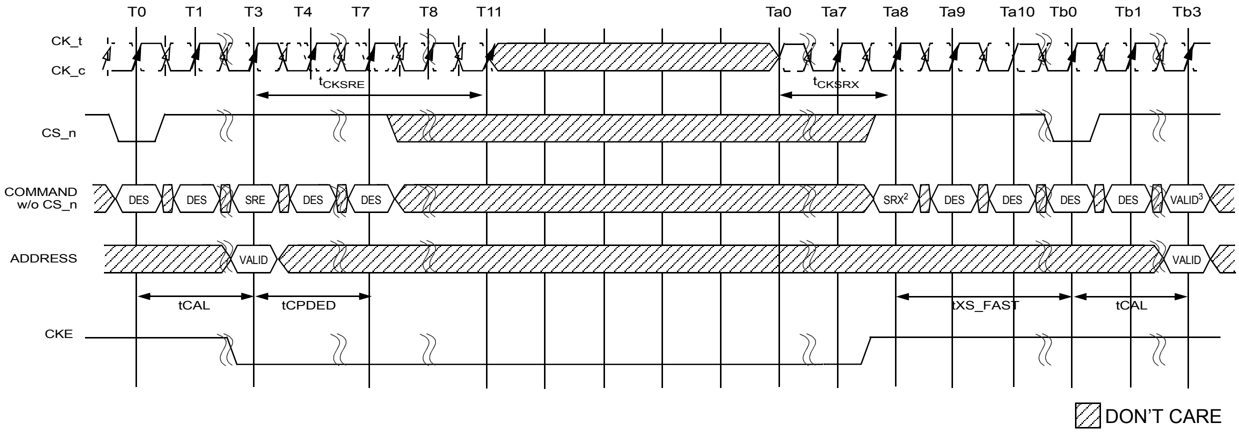
Figure 36. CAL enabling MRS to next MRS command, tMRD_CAL



NOTE :
1. MRS at Ta1 may or may not modify CAL, tMRD_CAL is computed based on new tCAL setting.
2. tMRD_CAL=tMOD+tCAL.

Figure 37. tMRD_CAL, mode register cycle time with CAL enabled

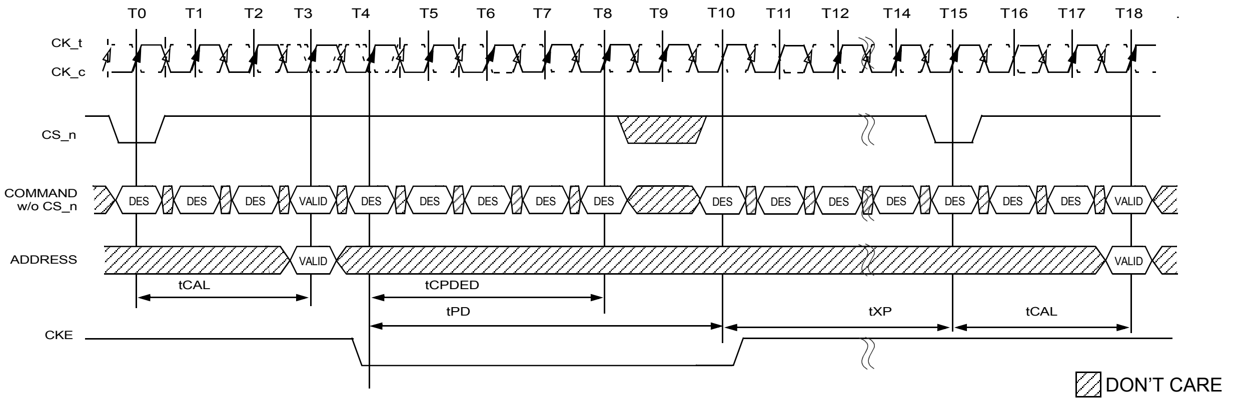
2.15.2 Self Refresh Entry, Exit Timing with CAL



NOTE:
1. tCAL = 3nCK, tCPDED = 4nCK, tCKSRE = 8nCK, tCKSRX = 8nCK, tXS_FAST = tRFC4(min) + 10ns
2. CS_n = H, ACT_n = Don't Care, RAS_n/A16 = Don't Care, CAS_n/A15 = Don't Care, WE_n/A14 = Don't Care
3. Only MRS (limited to those described in the Self-Refresh Operation section). ZQCS or ZQCL command allowed.

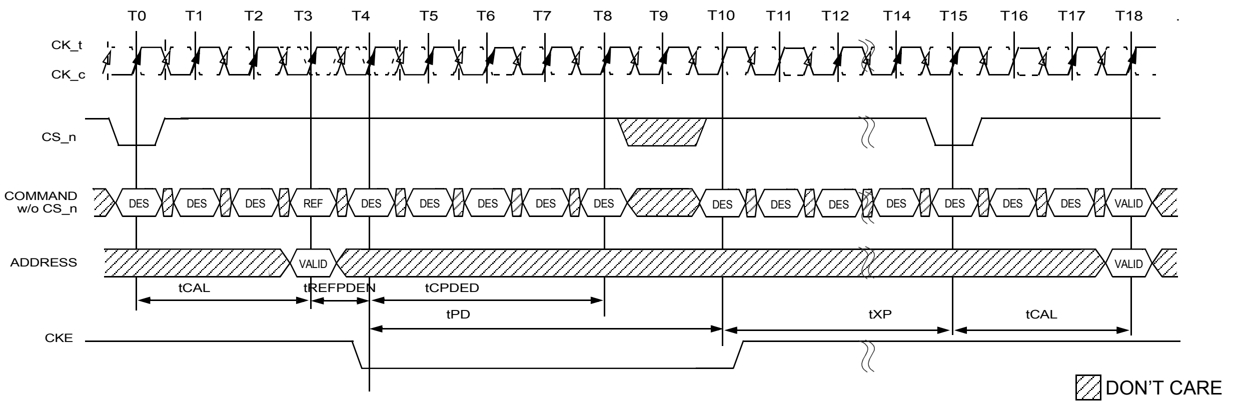
Figure 38. Self Refresh Entry/Exit Timing

2.15.3 Power Down Entry, Exit Timing with CAL



NOTE :
1. tCAL = 3nCK, tCPDED = 4nCK, tPD = 6nCK, tXP = 5nCK

Figure 39. Active Power Down Entry and Exit Timing



NOTE:
1. tCAL = 3nCK, tREFPDEN = 1nCK, tCPDED = 4nCK, tPD = 6nCK, tXP = 5nCK

Figure 40. Refresh Command to Power Down Entry

2.16 CRC

2.16.1 CRC Polynomial and logic equation

DDR4 supports CRC for write operation, and doesn't support CRC for read operation.
The CRC polynomial used by DDR4 is the ATM-8 HEC, X^8+X^2+X^1+1
A combinatorial logic block implementation of this 8-bit CRC for 72-bits of data contains 272 two-input XOR gates contained in eight 6 XOR gate deep trees.
The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.

[Table 50] Error Detection Details

ERROR TYPE	DETECTION CAPABILITY
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random one Multi-bit UI vertical column error detection excluding DBI bits	100%

CRC COMBINATORIAL LOGIC EQUATIONS

```
module CRC8_D72;
// polynomial: (0 1 2 8)
// data width: 72
// convention: the first serial data bit is D[71]
// initial condition all 0 implied
function [7:0]
nextCRC8_D72;
input [71:0] Data;
reg [71:0] D;
reg [7:0] NewCRC;
begin
D = Data;

NewCRC[0] = D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^
            D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
            D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
            D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
            D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;
NewCRC[1] = D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^
            D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
            D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
            D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
            D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
            D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] = D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^
            D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
            D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
            D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
            D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] = D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^
            D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
            D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
            D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
            D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
NewCRC[4] = D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^
            D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
            D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
            D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
            D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
NewCRC[5] = D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^
            D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
            D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
            D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
            D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];
NewCRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^
            D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
            D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
            D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
            D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];
NewCRC[7] = D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^
            D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
```

D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];

nextCRC8_D72 = NewCRC;

2.16.2 CRC data bit mapping for x8 devices

The following figure shows detailed bit mapping for a x8 device.

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	1
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	1
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	1
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	1
DQ4	d32	d33	d34	d35	d36	d37	d38	d39	CRC4	1
DQ5	d40	d41	d42	d43	d44	d45	d46	d47	CRC5	1
DQ6	d48	d49	d50	d51	d52	d53	d54	d55	CRC6	1
DQ7	d56	d57	d58	d59	d60	d61	d62	d63	CRC7	1
DBI_n	d64	d65	d66	d67	d68	d69	d70	d71	1	1

2.16.3 CRC data bit mapping for x4 devices

The following figure shows detailed bit mapping for a x4 device.

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	CRC4
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	CRC5
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	CRC6
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	CRC7

2.16.4 CRC data bit mapping for x16 devices

A x16 device is treated as two x8 devices. x16 device will have two identical CRC trees implemented. CRC(0-7) covers data bits d(0-71). CRC(8-15) covers data bits d(72-143).

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	1
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	1
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	1
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	1
DQ4	d32	d33	d34	d35	d36	d37	d38	d39	CRC4	1
DQ5	d40	d41	d42	d43	d44	d45	d46	d47	CRC5	1
DQ6	d48	d49	d50	d51	d52	d53	d54	d55	CRC6	1
DQ7	d56	d57	d58	d59	d60	d61	d62	d63	CRC7	1
DML_n/ DBIL_n	d64	d65	d66	d67	d68	d69	d70	d71	1	1
DQ8	d72	d73	d74	d75	d76	d77	d78	d79	CRC8	1
DQ9	d80	d81	d82	d83	d84	d85	d86	d87	CRC9	1
DQ10	d88	d89	d90	d91	d92	d93	d94	d95	CRC10	1
DQ11	d96	d97	d98	d99	d100	d101	d102	d103	CRC11	1
DQ12	d104	d105	d106	d107	d108	d109	d110	d111	CRC12	1
DQ13	d112	d113	d114	d115	d116	d117	d118	d119	CRC13	1
DQ14	d120	d121	d122	d123	d124	d125	d126	d127	CRC14	1
DQ15	d128	d129	d130	d131	d132	d133	d134	d135	CRC15	1
DMU_n/ DBIU_n	d136	d137	d138	d139	d140	d141	d142	d143	1	1

2.16.5 Write CRC for x4, x8 and x16 devices

The Controller generates the CRC checksum and forms the write data frames as shown in Section 2.16.1 to Section 2.16.4.

For a x8 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the DBI_n lane if DBI function is enabled.

For a x16 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the DBIL_n and DBIU_n lanes if DBI function is enabled.

The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the ALERT_n signal if there is a mis-match.

A x8 device has a CRC tree with 72 input bits. The upper 8 bits are used if either Write DBI or DM is enabled. Note that Write DBI and DM function cannot be enabled simultaneously. If both Write DBI and DM is disabled then the inputs of the upper 8 bits D[71:64] are '1's.
.

A x16 device has two identical CRC trees with 72 input bits each. The upper 8 bits are used for DBI inputs if DBI is enabled. If DBI is disabled then the input of the upper 8 bits [D(143:136) and D(71:64)] is '1'.

A x4 device has a CRC tree with 32 input bits. The input for the upper 40 bits D[71:32] are '1's.

DRAM can write data to the DRAM core without waiting for CRC check for full writes. If bad data is written to the DRAM core then controller will retry the transaction and overwrite the bad data. Controller is responsible for data coherency.

2.16.6 CRC Error Handling

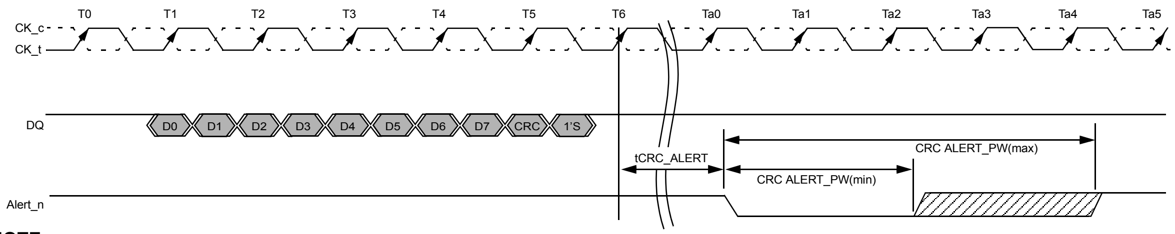
CRC Error mechanism shares the same Alert_n signal for reporting errors on writes to DRAM. The controller has no way to distinguish between CRC errors and Command/Address/Parity errors other than to read the DRAM mode registers. This is a very time consuming process in a multi-rank configuration.

To speed up recovery for CRC errors, CRC errors are only sent back as a pulse. The minimum pulse-width is 6 clocks. The latency to Alert_n signal is defined as tCRC_ALERT in the figure below.

DRAM will set CRC Error Clear bit in A3 of MR5 to '1' and CRC Error Status bit in MPR3 of page1 to '1' upon detecting a CRC error. The CRC Error Clear bit remains set at '1' until the host clears it explicitly using an MRS command.

The controller upon seeing an error as a pulse width will retry the write transactions. The controller understands the worst case delay for Alert_n (during init) and can backup the transactions accordingly or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than six clocks at the controller if there are multiple CRC errors as the Alert_n is a daisy chain bus.



NOTE :
1. CRC ALERT_PW is specified from the point where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up.
2. Timing diagram applies to x4, x8, and x16 devices.

Figure 41. CRC Error Reporting

[Table 51] CRC Error Timing Parmeters

Parameter	Symbol	DDR4-1600 min	DDR4-1600 max	DDR4-1866 min	DDR4-1866 max	DDR4-2133 min	DDR4-2133 max	DDR4-2400 min	DDR4-2400 max	Unit
CRC error to ALERT_n latency	tCRC_ALERT	-	13	-	13	-	13	-	13	ns
CRC ALERT_n pulse width	CRC ALERT_PW	6	10	6	10	6	10	6	10	nCK

2.16.7 CRC Frame format with BC4

DDR4 SDRAM supports CRC function for Write operation for Burst Chop 4 (BC4). The CRC function is programmable using DRAM mode register and can be enabled for writes.

When CRC is enabled the data frame length is fixed at 10UI for both BL8 and BC4 operations. DDR4 SDRAM also supports burst length on the fly with CRC enabled. This is enabled using mode register.

CRC data bit mapping for x4 devices (BC4)
The following figure shows detailed bit mapping for a x4 device.

	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	CRC4
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	CRC5
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	CRC6
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	CRC7

For a x4 SDRAM, the CRC tree input is 16 data bits as shown in the figure above. The input for the remaining bits are “1”.

CRC data bit mapping for x8 devices (BC4)
The following figure shows detailed bit mapping for a x8 device.

	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	1
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	1
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	1
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	1
DQ4	d32	d33	d34	d35	1	1	1	1	CRC4	1
DQ5	d40	d41	d42	d43	1	1	1	1	CRC5	1
DQ6	d48	d49	d50	d51	1	1	1	1	CRC6	1
DQ7	d56	d57	d58	d59	1	1	1	1	CRC7	1
DM_n DBI_n	d64	d65	d66	d67	1	1	1	1	1	1

For a x8 SDRAM, the CRC tree inputs are 36 bits as shown in the figure above. The input bits d(64:67) are used if DBI or DM functions are enabled. If DBI and DM are disabled then d(64:67) are “1”

CRC data bit mapping for x16 devices (BC4)
The following figure shows detailed bit mapping for a x16 device.

	Tranfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	1
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	1
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	1
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	1
DQ4	d32	d33	d34	d35	1	1	1	1	CRC4	1
DQ5	d40	d41	d42	d43	1	1	1	1	CRC5	1
DQ6	d48	d49	d50	d51	1	1	1	1	CRC6	1
DQ7	d56	d57	d58	d59	1	1	1	1	CRC7	1
DML_n DBIL_n	d64	d65	d66	d67	1	1	1	1	1	1
DQ8	d72	d73	d74	d75	1	1	1	1	CRC8	1
DQ9	d80	d81	d82	d83	1	1	1	1	CRC9	1
DQ10	d88	d89	d90	d91	1	1	1	1	CRC10	1
DQ11	d96	d97	d98	d99	1	1	1	1	CRC11	1
DQ12	d104	d105	d106	d107	1	1	1	1	CRC12	1
DQ13	d112	d113	d114	d115	1	1	1	1	CRC13	1
DQ14	d120	d121	d122	d123	1	1	1	1	CRC14	1
DQ15	d128	d129	d130	d131	1	1	1	1	CRC15	1
DMU_n DBIU_n	d136	d137	d138	d139	1	1	1	1	1	1

For a x16 SDRAM there are two identical CRC trees.
The lower CRC tree inputs has 36 bits as shown in the figure above. The input bits d(64:67) are used if DBI or DM functions are enabled. If DBI and DM are disabled then d(64:67) are “1”.
The upper CRC tree inputs has 36 bits as shown in the figure above. The input bits d(136:139) are used if DBI or DM functions are enabled. If DBI and DM are disabled then d(136:139) are “1”.

DBI and CRC clarification
Write operation: The SDRAM computes the CRC for received data d(71:0). Data is not inverted based on DBI before it is used for computing CRC. The data is inverted based on DBI before it is written to the DRAM core.

Burst Ordering with BC4 and CRC enabled
If CRC is enabled then address bit A2 is used to transfer critical data first for BC4 writes.
A x8 SDRAM is used as an example with DBI enabled.
The following figure shows data frame with A2=0.

	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	1
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	1
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	1
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	1
DQ4	d32	d33	d34	d35	1	1	1	1	CRC4	1
DQ5	d40	d41	d42	d43	1	1	1	1	CRC5	1
DQ6	d48	d49	d50	d51	1	1	1	1	CRC6	1
DQ7	d56	d57	d58	d59	1	1	1	1	CRC7	1
DM_n DBI_n	d64	d65	d66	d67	1	1	1	1	1	1

The following figure shows data frame with A2=1.

	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	d4	d5	d6	d7	1	1	1	1	CRC0	1
DQ1	d12	d13	d14	d15	1	1	1	1	CRC1	1
DQ2	d20	d21	d22	d23	1	1	1	1	CRC2	1
DQ3	d28	d29	d30	d31	1	1	1	1	CRC3	1
DQ4	d36	d37	d38	d39	1	1	1	1	CRC4	1
DQ5	d44	d45	d46	d47	1	1	1	1	CRC5	1
DQ6	d52	d53	d54	d55	1	1	1	1	CRC6	1
DQ7	d60	d61	d62	d63	1	1	1	1	CRC7	1
DM_n DBI_n	d68	d69	d70	d71	1	1	1	1	1	1

If A2=1 then the data input to the CRC tree are 36 bits as shown above. Data bits d(4:7) are used as inputs for d(0:3), d(12:15) are used as inputs to d(8:11) and so forth for the CRC tree.
The input bits d(68:71) are used if DBI or DM functions are enabled. If DBI and DM are disabled then d(68:71) are "1"s. If A2=1 then data bits d(68:71) are used as inputs for d(64:67)
The CRC tree will treat the 36 bits in transfer's four through seven as 1's

CRC equations for x8 device in BC4 mode with A2=0 are as follows:

CRC[0] = D[69]=1 ^ D[68]=1 ^ D[67] ^ D[66] ^ D[64] ^ D[63]=1 ^ D[60]=1 ^ D[56] ^ D[54]=1 ^ D[53]=1 ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^ D[45]=1 ^ D[43] ^ D[40] ^ D[39]=1 ^ D[35] ^ D[34] ^ D[31]=1^ D[30]=1 ^ D[28]=1 ^ D[23]=1 ^ D[21]=1 ^ D[19] ^ D[18] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[8] ^ D[7]=1 ^ D[6] =1 ^ D[0] ;
CRC[1] = D[70]=1 ^ D[66] ^ D[65] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^D[56] ^ D[55]=1 ^ D[52]=1 ^ D[51] ^ D[48] ^ D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[43] ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[34] ^ D[32] ^ D[30]=1 ^ D[29]=1 ^ D[28]=1 ^ D[24] ^ D[23]=1 ^ D[22]=1 ^ D[21]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[16] ^ D[15]=1 ^ D[14]=1 ^ D[13]=1 ^ D[12]=1 ^ D[9] ^ D[6]=1 ^ D[1] ^ D[0];
CRC[2] = D[71]=1 ^ D[69]=1 ^ D[68]=1 ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[60]=1 ^ D[58] ^ D[57] ^ D[54]=1 ^ D[50] ^ D[48] ^ D[47]=1 ^ D[46]=1 ^ D[44]=1 ^ D[43] ^ D[42] ^ D[39]=1 ^ D[37]=1 ^ D[34] ^ D[33] ^ D[29]=1 ^ D[28]=1 ^ D[25] ^ D[24] ^ D[22]=1 ^ D[17] ^ D[15]=1 ^ D[13]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[6]=1 ^ D[2] ^ D[1] ^ D[0];
CRC[3] = D[70]=1 ^ D[69]=1 ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[59] ^ D[58] ^ D[55]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^ D[45]=1 ^ D[44]=1 ^ D[43] ^ D[40] ^ D[38]=1 ^ D[35] ^ D[34] ^ D[30]=1 ^ D[29]=1 ^ D[26] ^ D[25] ^ D[23]=1 ^ D[18] ^ D[16] ^ D[14]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[7]=1 ^ D[3] ^ D[2] ^ D[1];
CRC[4] = D[71]=1 ^ D[70]=1 ^ D[65] ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[60]=1 ^ D[59] ^ D[56] ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^ D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[35] ^ D[31]=1 ^ D[30]=1 ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15]=1 ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[4]=1 ^ D[3] ^ D[2];
CRC[5] = D[71]=1 ^ D[66] ^ D[65] ^ D[64] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^ D[53]=1 ^ D[51] ^ D[50] ^ D[49] ^ D[47]=1 ^ D[46]=1 ^ D[45]=1 ^ D[42] ^ D[40] ^ D[37]=1 ^ D[36]=1 ^ D[32] ^ D[31]=1 ^ D[28]=1 ^ D[27] ^ D[25] ^ D[20]=1 ^ D[18] ^ D[16] ^ D[15]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[5]=1 ^ D[4]=1 ^ D[3];
CRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62]=1 ^ D[61]=1 ^ D[58] ^ D[54]=1 ^ D[52]=1 ^ D[51] ^ D[50] ^ D[48] ^ D[47]=1 ^ D[46]=1 ^ D[43] ^ D[41] ^ D[38]=1 ^ D[37]=1 ^ D[33] ^ D[32] ^ D[29]=1 ^ D[28]=1 ^ D[26] ^ D[21]=1 ^ D[19] ^ D[17] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[6]=1 ^ D[5]=1 ^ D[4]=1;
CRC[7] = D[68]=1 ^ D[67] ^ D[66] ^ D[65] ^ D[63]=1 ^ D[62]=1 ^ D[59] ^ D[55]=1 ^ D[53]=1 ^ D[52]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^ D[44]=1 ^ D[42] ^ D[39]=1 ^ D[38]=1 ^ D[34] ^ D[33] ^ D[30]=1 ^ D[29]=1 ^ D[27] ^ D[22]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[15] =1^ D[13]=1 ^ D[11] ^ D[7]=1 ^ D[6]=1 ^ D[5]=1;

CRC equations for x8 device in BC4 mode with A2=1 are as follows:

CRC[0] = 1 ^ 1 ^ D[71] ^ D[70] ^ D[68] ^ 1 ^ 1 ^ D[60] ^ 1 ^ 1 ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1^ 1 ^ 1 ^ 1 ^ 1 ^ D[23] ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[12] ^ 1 ^ 1 ^ D[4] ;
CRC[1] = 1 ^ D[70] ^ D[69] ^ 1 ^ 1 ^ 1 ^ D[61] ^ D[60] ^ 1 ^ 1 ^ D[55] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[38] ^ D[36] ^ 1 ^ 1 ^ 1 ^ D[28] ^ 1 ^ 1 ^ 1 ^ 1 ^ D[22] ^ D[21] ^ D[20] ^1 ^ 1 ^1 ^ 1 ^ D[13] ^ 1 ^ D[5] ^ D[4];
CRC[2] = 1 ^ 1 ^ 1 ^1 ^1 ^ 1 ^ 1 ^ D[62] ^ D[61] ^ 1 ^ D[54] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[29] ^ D[28] ^ 1 ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D12] ^1 ^ D[6] ^ D[5] ^ D[4];
CRC[3] = 1 ^ 1 ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[62] ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1 ^ 1 ^ D[30] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ D[7] ^ D[6] ^ D[5];
CRC[4] = 1 ^1 ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[60] ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^1 ^ 1 ^ D[45] ^ 1 ^ 1 ^ D[39] ^1 ^ 1 ^ D[31] ^ D[30] ^ D[28] ^ D[23] ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D[12] ^ 1 ^ D[7] ^ D[6];
CRC[5] = 1 ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[61] ^ 1 ^ D[55] ^ D[54] ^ D[53] ^ 1 ^ 1 ^ 1 ^ D[46] ^ D[44] ^ 1 ^ 1 ^ D[36] ^ 1 ^ 1 ^ D[31] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ 1 ^ D[7];
CRC[6] = D[71] ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ D[62] ^ 1 ^ 1 ^ D[55] ^ D[54] ^ D[52] ^ 1 ^1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^

D[37] ^ D[36] ^1 ^ 1 ^ D[30] ^ 1 ^ D[23] ^ D[21] ^ D[20] ^ 1 ^ 1 ^ D[14] ^ 1 ^ 1 ^ 1;

CRC[7] = 1 ^ D[71] ^ D[70] ^ D[69] ^ 1 ^ 1 ^ D[63] ^ 1 ^ 1 ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[31] ^ 1 ^ 1 ^ D[22] ^ D[21] ^ 1^ 1 ^ D[15] ^ 1 ^ 1 ^ 1;

2.16.8 Simultaneous DM and CRC Functionality

When both DM and Write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array. If there is a CRC error, the DRAM blocks the write operation and discards the data.

2.16.9 Simultaneous MPR Write, Per DRAM Addressability and CRC Functionality

The following combination of DDR4 features are prohibited for simultaneous operation

1) MPR Write and Write CRC (Note: MPR Write is via Address pins)

C/A Parity signal (PAR) covers ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14 the address bus including bank address and bank group bits, and C0-C2 on 3DS devices. The control signals CKE, ODT and CS_n are not included. (e.g. for a 4 Gbit x4 monolithic device, parity is computed across BG0, BG1, BA1, BA0, A16/ RAS_n, A15/CAS_n, A14/WE_n, A13-A0 and ACT_n). (DRAM should internally treat any unused address pins as 0's, e.g., if a common die has stacked pins but the device is used in a monolithic application then the address pins used for stacking should internally be treated as 0's)

· Ignore the erroneous command. Commands in max NnCK window (tPAR_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a READ command in this NnCK window is not executed, the DRAM does not activate DQS outputs.

· Log the error by storing the erroneous command and address bits in the error log. (MPR page1)

· Set the Parity Error Status bit in the mode register to '1'. The Parity Error Status bit must be set before the ALERT_n signal is released by the DRAM (i.e. tPAR_ALERT_ON + tPAR_ALERT_PW(min)).

· Assert the ALERT_n signal to the host (ALERT_n is active low) within tPAR_ALERT_ON time.

2.17 Command Address Parity(CA Parity)

[A2:A0] of MR5 are defined to enable or disable C/A Parity in the DRAM. The default state of the C/A Parity bits is disabled. If C/A parity is enabled by programming a non-zero value to C/A Parity Latency in the mode register (the Parity Error bit must be set to zero when enabling C/A any Parity mode), then the DRAM has to ensure that there is no parity error before executing the command. The additional delay for executing the commands versus a parity disabled mode is programmed in the mode register(MR5, A2:A0) when C/A Parity is enabled (PL:Parity Latency) and is applied to all commands.The command is held for the time of the Parity Latency before it is executed inside the device. This means that issuing timing of internal command is determined with PL. When C/A Parity is enabled, only DES is allowed between valid commands to prevent DRAM from any malfunctioning. CA Parity Mode is supported when DLL-on Mode is enabled, use of CA Parity Mode when DLL-off Mode is enabled is not allowed.

C/A Parity signal (PAR) covers ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14 and the address bus including bank address and bank group bits, and C0-C2 on 3DS devices. The control signals CKE, ODT and CS_n are not included. (e.g. for a 4 Gbit x4 monolithic device, parity is computed across BG0, BG1, BA1, BA0, A16/ RAS_n, A15/CAS_n, A14/WE_n, A13-A0 and ACT_n). (DRAM should internally treat any unused address pins as 0's, e.g. if a common die has stacked pins but the device is used in a monolithic application then the address pins used for stacking should internally be treated as 0's)

The convention of parity is even parity i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity bit is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even.

If a DRAM detects a C/A parity error in any command as qualified by CS_n then it must perform the following steps:

· Ignore the erroneous command. Commands in max NnCK window (tPAR_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a READ command in this NnCK window is not executed, the DRAM does not activate DQS outputs.

· Log the error by storing the erroneous command and address bits in the error log. (MPR page1)

· Set the Parity Error Status bit in the mode register to '1'. The Parity Error Status bit must be set before the ALERT_n signal is released by the DRAM (i.e. tPAR_ALERT_ON + tPAR_ALERT_PW(min)).

· Assert the ALERT_n signal to the host (ALERT_n is active low) within tPAR_ALERT_ON time.

· Wait for all in-progress commands to complete. These commands were received tPAR_UNKOWN before the erroneous command.
If a parity error occurs on a command issued between the tXS_Fast and tXS window after self-refresh exit then the DRAM may delay the de-assertion of ALERT_n signal as a result of any internal on going refresh. (See Figure 46)

· Wait for tRAS_min before closing all the open pages. The DRAM is not executing any commands during the window defined by (tPAR_ALERT_ON + tPAR_ALERT_PW).

· After tPAR_ALERT_PW_min has been satisfied, the DRAM may de-assert ALERT_n.

· After the DRAM has returned to a known pre-charged state it may de-assert ALERT_n.

· After (tPAR_ALERT_ON + tPAR_ALERT_PW), the DRAM is ready to accept commands for normal operation. Parity latency will be in effect, however, parity checking will not resume until the memory controller has cleared the Parity Error Status bit by writing a '0'(the DRAM will execute any erroneous commands until the bit is cleared).

· It is possible that the DRAM might have ignored a refresh command during the (tPAR_ALERT_ON + tPAR_ALERT_PW) window or the refresh command is the first erroneous frame so it is recommended that the controller issues extra refresh cycles as needed.

· The Parity Error Status bit may be read anytime after (tPAR_ALERT_ON + tPAR_ALERT_PW) to determine which DRAM had the error. The DRAM maintains the Error Log for the first erroneous command until the Parity Error Status bit is reset to '0'.

Mode Register for C/A Parity Error is defined as follows. C/A Parity Latency bits are write only, Parity Error Status bit is read/write and error logs are read only bits. The controller can only program the Parity Error Status bit to '0'. If the controller illegally attempts to write a '1' to the Parity Error Status bit the DRAM does not guarantee that parity will be checked. The DRAM may opt to block the controller from writing a '1' to the Parity Error Status bit.

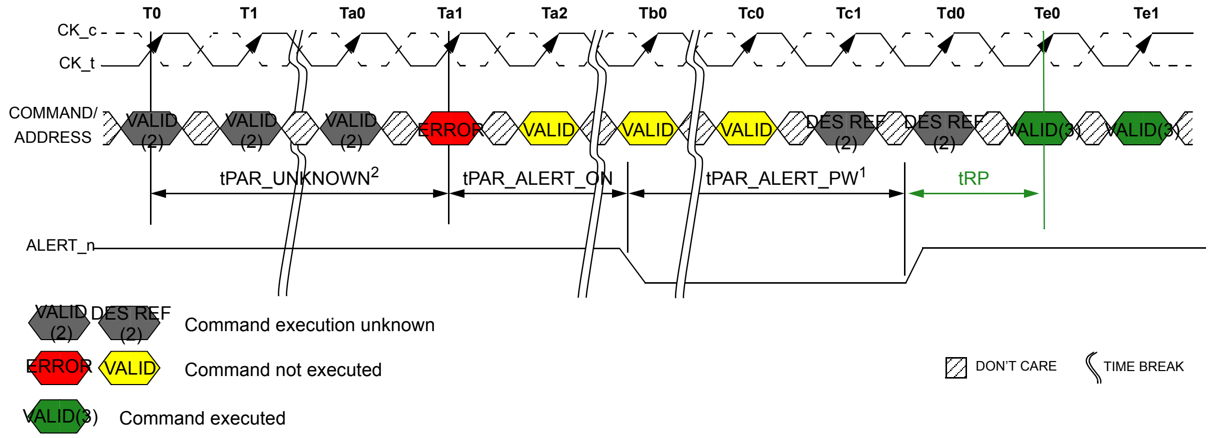
[Table 52] Mode Registers for C/A Parity

C/A Parity Latency MR5[2:0]*	Speed bins	C/A Parity Error Status MR5[4]	Errant C/A Frame
000 = Disabled	-	0=clear	C2-C0, ACT_n, BG1, BG0, BA0, BA1, PAR, A17, A16/ RAS_n, A15/CAS_n, A14/WE_n, A13:A0
001= 4 Clocks	1600,1866,2133		
010= 5 Clocks	2400	1=Error	
011= 6 Clocks	RFU		
100= 8 Clocks	RFU		

NOTE :
1. Parity Latency is applied to all commands.
2. Parity Latency can be changed only from a C/A Parity disabled state, i.e. a direct change from PL=4 → PL=5 is not allowed. Correct sequence is PL=4 → Disabled → PL=5
3. Parity Latency is applied to write and read latency. Write Latency = AL+CWL+PL. Read Latency = AL+CL+PL.

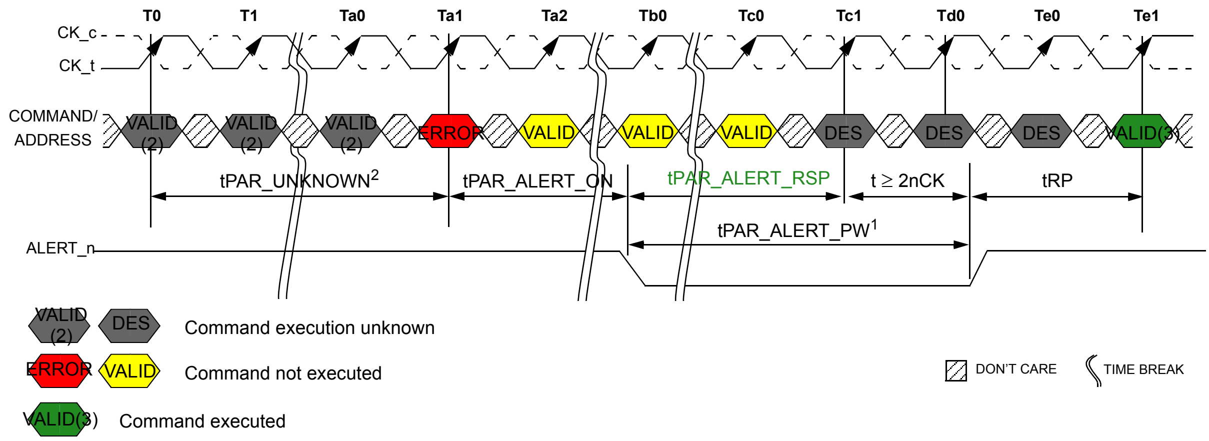
DDR4 SDRAM supports MR bit for ‘Persistent Parity Error Mode’. This mode is enabled by setting MR5 A9=High and when it is enabled, DRAM resumes checking CA Parity after the alert_n is deasserted, even if Parity Error Status bit is set as High. If multiple errors occur before the Error Status bit is cleared the Error log in MPR page 1 should be treated as ‘Don’t Care’. In ‘Persistent Parity Error Mode’ the Alert_n pulse will be asserted and deasserted by the DRAM as defined with the min. and max. value for tPAR_ALERT_PW. The controller must issue DESELECT commands com-mands once it detects the Alert_n signal, this response time is defined as tPAR_ALERT_RSP

The following figure captures the flow of events on the C/A bus and the ALERT_n signal.



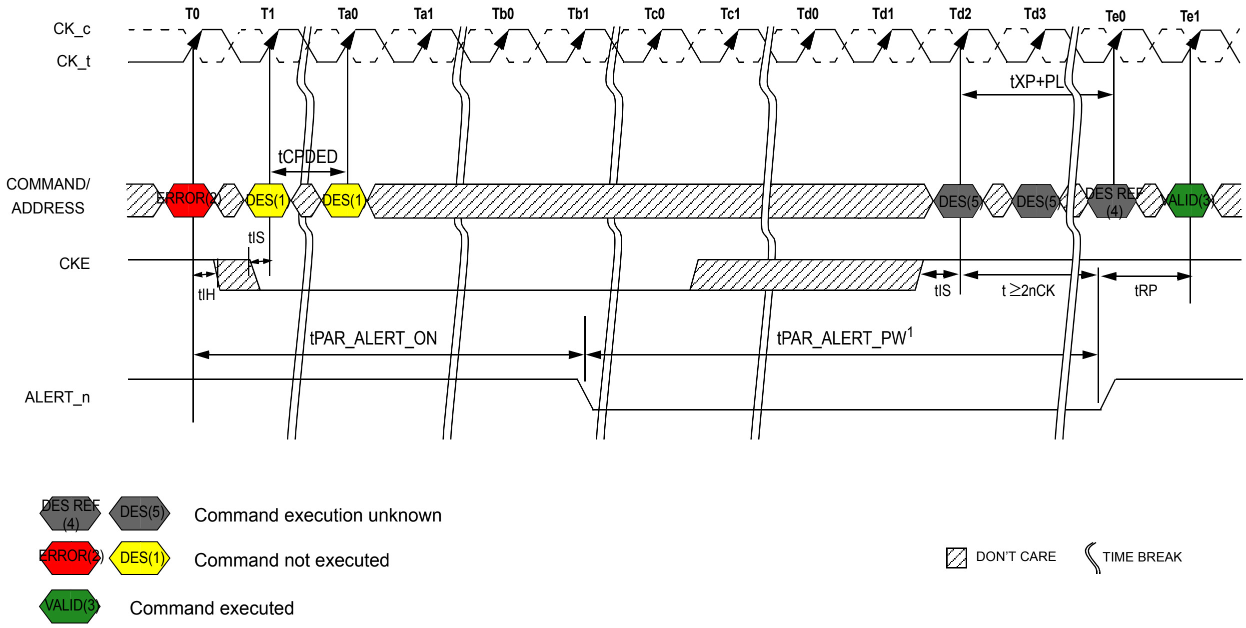
NOTE :
1. DRAM is emptying queues, Precharge All and parity checking off until Parity Error Status bit cleared.
2. Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.
3. Normal operation with parity latency(CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.

Figure 42. Normal CA Parity Error Checking Operation



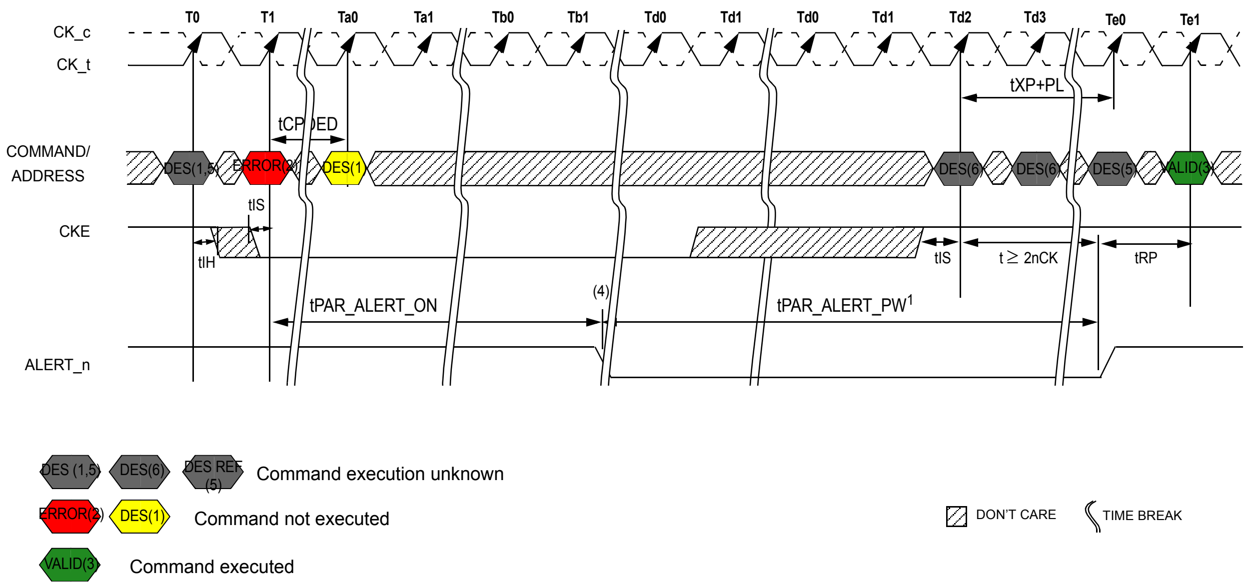
NOTE :
1. DRAM is emptying queues, Precharge All and parity check re-enable finished by tPAR_ALERT_PW.
2. Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.
3. Normal operation with parity latency and parity checking (CA Parity Persistent Error Mode enabled).

Figure 43. Persistent CA Parity Error Checking Operation



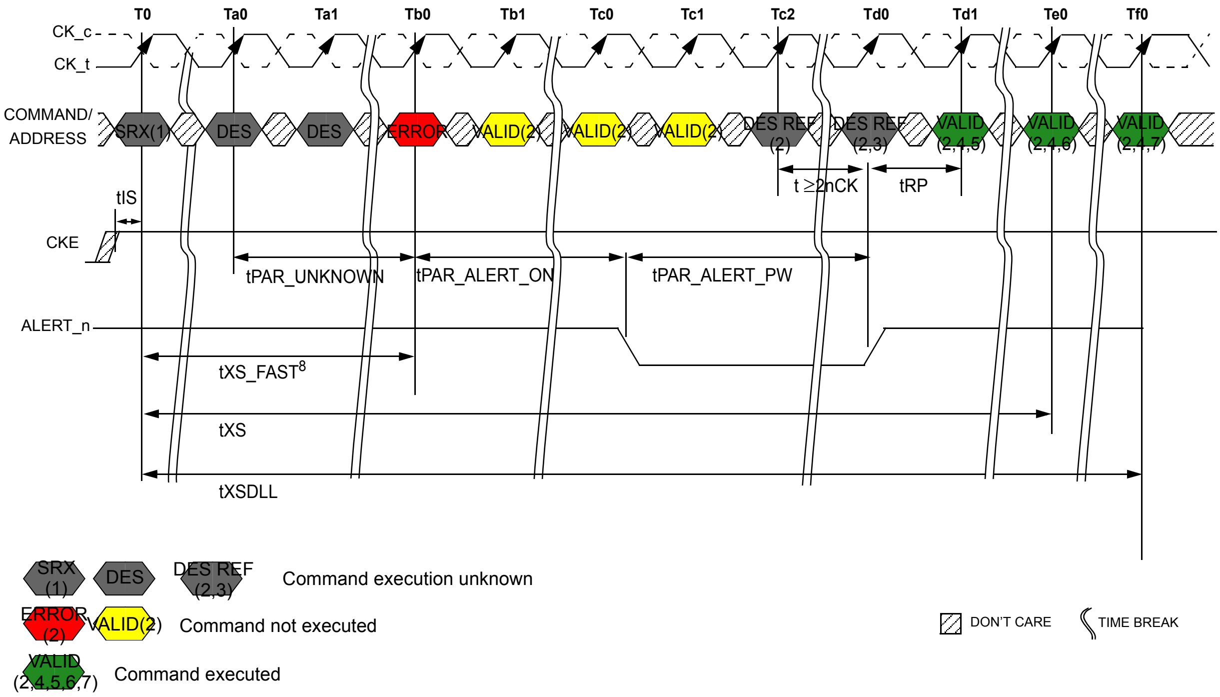
NOTE :
1. Deselect command only only allowed.
2. Error could be Precharge or Activate.
3. Normal operation with parity latency(CA Parity Persistent Error Mode disable). Parity checking is off until Parity Error Status bit cleared.
4. Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.
5. Deselect command only allowed CKE may go high prior to Td2 as long as DES commands are issued.

Figure 44. CA Parity Error Checking - PDE/PDX



NOTE :
1. Deselect command only only allowed.
2. SelfRefresh command error. DRAM masks the intended SRE cammand enters Precharge Down.
3. Normal operation with parity latency(CA Parity Persistent Error Mode disable). Parity checking is off until Parity Error Status bit cleared.
4. Controller can not disable clock until it has been able to have detected a possible C/A Parity error.
4. Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.
5. Deselect command only allowed CKE may go high prior to Tc2 as long as DES commands are issued.

Figure 45. CA Parity Error Checking - SRE Attempt



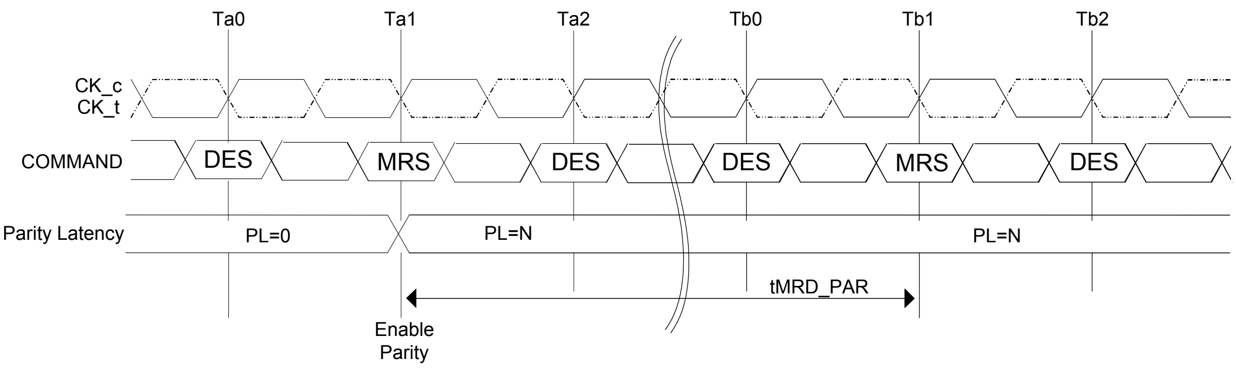
NOTE :
1. SelfRefresh Abort = Disable : MR4 [A9=0]
2. Input commands are bounded by tXSDLL, tXS, tXS_ABORT and tXS_FAST timing.
3. Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.
4. Normal operation with parity latency(CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.
5. Only MRS (limited to those described in the Self-Refresh Operation section), ZQCS or ZQCL command allowed.
6. Valid commands not requiring a locked DLL
7. Valid commands requiring a locked DLL
8. This figure shows the case from which the error occurred after tXS FAST_An error also occur after tXS_ABORT and tXS.

Figure 46. CA Parity Error Checking - SRX

Command/Address parity entry and exit timings

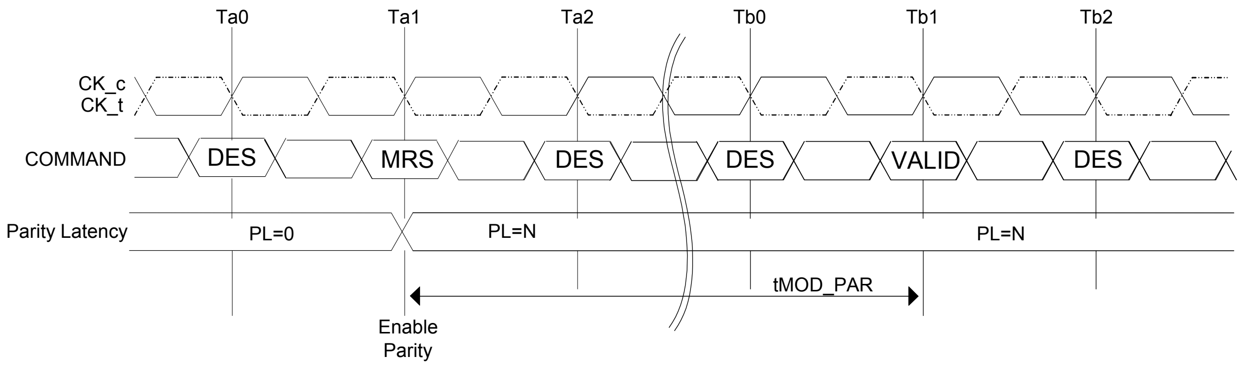
When in CA Parity mode, including entering and exiting CA Parity mode, users must wait tMRD_PAR before issuing another MRS command, and wait tMOD_PAR before any other commands.

tMOD_PAR = tMOD + PL
tMRD_PAR = tMOD + PL
For CA parity entry, PL in the equations above is the parity latency programmed with the MRS command entering CA parity mode.
For CA parity exit, PL in the equations above is the programmed parity latency prior to the MRS command exiting CA parity mode.



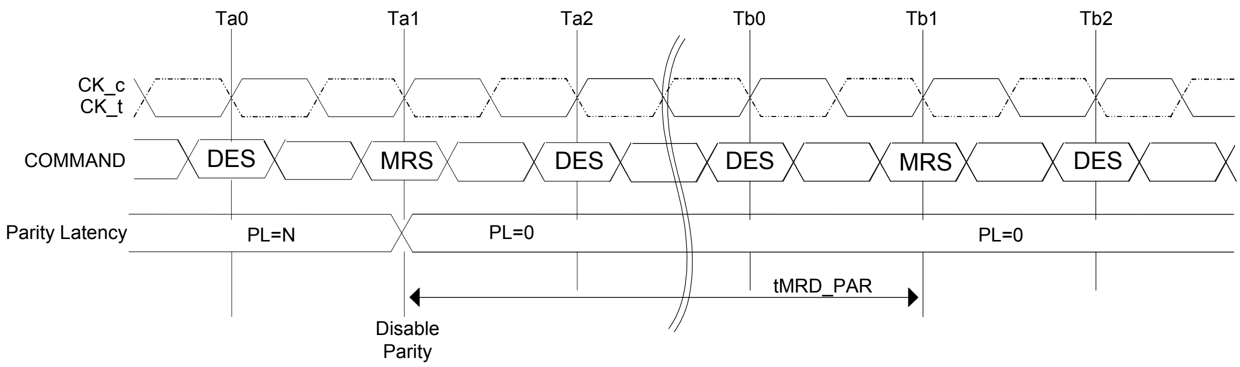
NOTE :
1. tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Figure 47. Parity entry timing example - tMRD_PAR



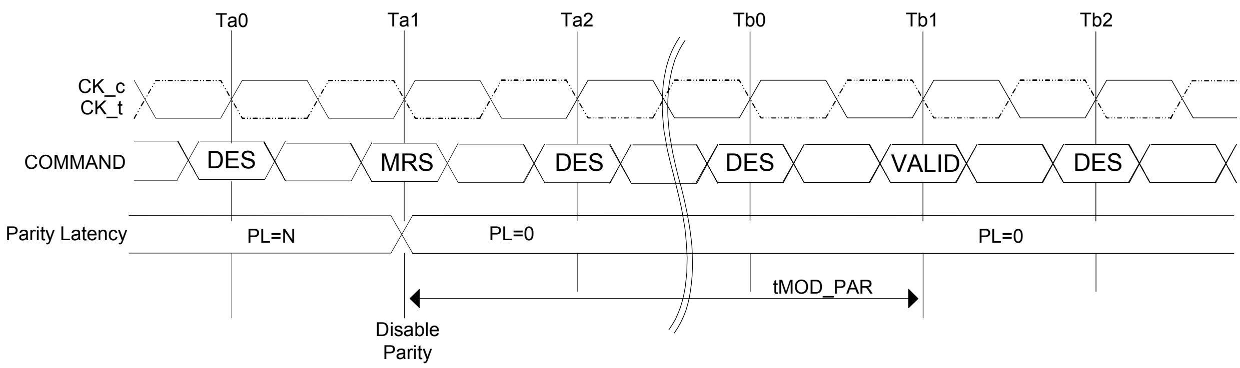
NOTE :
1. tMOD_PAR = tMOD + N; where N is the programmed parity latency.

Figure 48. Parity entry timing example - tMOD_PAR



NOTE :
1. tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Figure 49. Parity exit timing example - tMRD_PAR



NOTE :
1. tMOD_PAR = tMOD + N; where N is the programmed parity latency.

Figure 50. Parity exit timing example - tMOD_PAR

2.17.1 CA Parity Error Log Readout

MPR Mapping of CA Parity Error Log[1](Page1)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BA1:BA0 = 0:1	00=MPR0	A7	A6	A5	A4	A3	A2	A1	A0
	01=MPR1	CAS_n/A15	WE_n/A14	A13	A12	A11	A10	A9	A8
	10=MPR2	PAR	ACT_n	BG1	BG0	BA1	BA0	A17	RAS_n/ A16
	11=MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency			C2	C1	C0

NOTE :
1. MPR used for CA parity error log readout is enabled by setting A[2] in MR3
2. For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.
3. If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

2.18 Control Gear-down Mode

The following description represents the sequence for the gear-down mode which is specified with MR3:A3. This mode is allowed just during initialization and self refresh exit. The DRAM defaults in 1/2 rate(1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE and ODT in 1/4rate(2N) mode. For operation in 1/2 rate mode MRS command for geardown or sync pulse are not required. DRAM defaults in 1/2 rate mode.

General sequence for operation in geardown during initialization
- DRAM defaults to a 1/2 rate(1N mode) internal clock at power up/reset
- Assertion of Reset
- Assertion of CKE enables the DRAM
- MRS is accessed with a low frequency N*tck MRS geardown CMD (set MR3:A3 to 1
  Ntck static MRS command qualified by 1N CS_n
- DRAM controller sends 1N sync pulse with a low frequency N*tck NOP CMD
  tSYNC_GEAR is an even number of clocks
  Sync pulse on even clock boundary from MRS CMD
- Initialization sequence, including the expiration of tDLLK and tZQinit, starts
  in 2N mode after tCMD_GEAR from 1N Sync Pulse.

General sequence for operation in gear-down after self refresh exit
- DRAM reset to 1N mode during self refresh
- MRS is accessed with a low frequency N*tck MRS gear-down CMD (set MR3:A3 to 1)
  Ntck static MRS command qualified by 1N CS_n which meets tXS or tXS_Abort
  Only Refresh command is allowed to be issued to DRAM before Ntck static MRS command
- DRAM controller sends 1N sync pulse with a low frequency N*tck NOP CMD

tSYNC_GEAR is an even number of clocks
Sync pulse is on even clock boundary from MRS CMD
-Valid command not requiring locked DLL is available in 2N mode after tCMD_GEAR from 1N Sync Pulse.
-Valid command requiring locked DLL is available in 2N mode after tDLLK from 1N Sync Pulse

If operation is 1/2 rate(1N) mode after self refresh, no N*tCK MRS command or sync pulse is required during self refresh exit.
The min exit delay is tXS, or tXS_Abort to the first valid command.

The DRAM may be changed from 1/4 rate (2N) to 1/2 rate (1N) by entering Self Refresh Mode, which will reset to 1N automatically.
Changing from 1/4 (2N) to 1/2 rate (1 N) by any other means, including setting MR3[A3] from 1 to 0, can result in loss of data and operation of the DRAM uncertain.

For the operation of geardown mode in 1/4 rate, the following MR settings should be applied.

CAS Latency (MR0 A[6:4,2]) : Even number of clocks

Write Recovery and Read to Precharge (MR0 A[11:9]) : Even number of clocks

Additive Latency (MR1 A[4:3]) : 0, CL -2

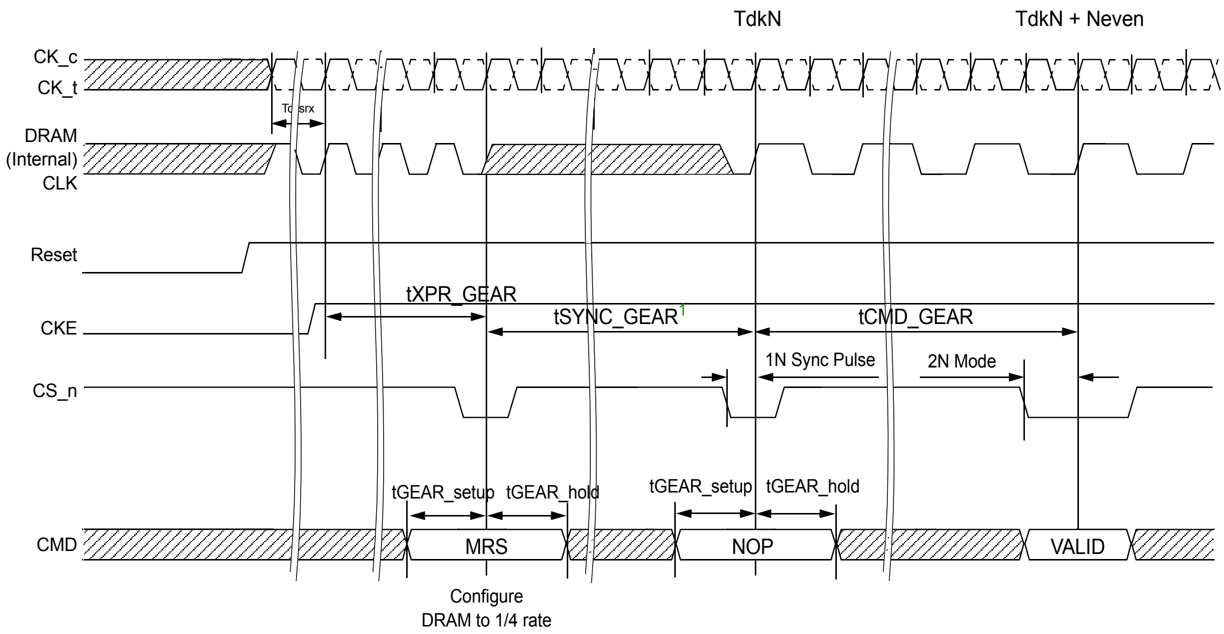
CAS Write Latency (MR2 A[5:3]) : Even number of clocks

CS to Command/Address Latency Mode (MR4 A[8:6]) : Even number of clocks

CA Parity Latency Mode (MR5 A[2:0]) : Even number of clocks

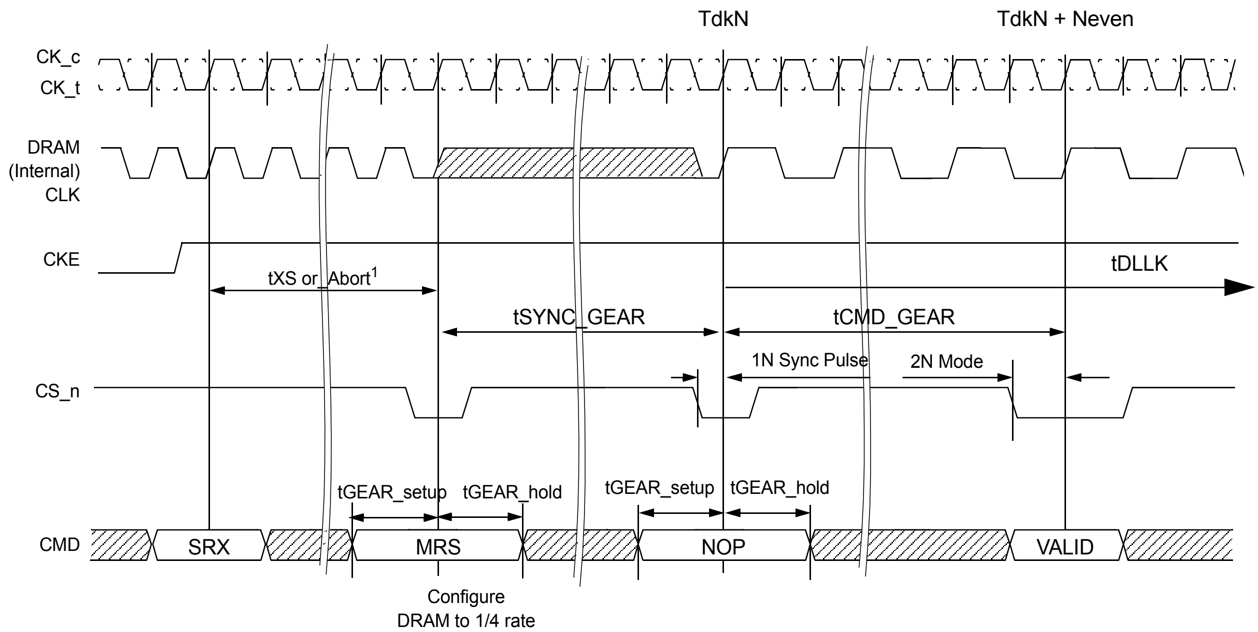
CAL or CA parity mode must be disabled prior to Gear down MRS command. They can be enabled again after tSYNC_GEAR and tCMD_GEAR periods are satisfied.

The diagram below illustrates the sequence for control operation in 2N mode during intialization. .



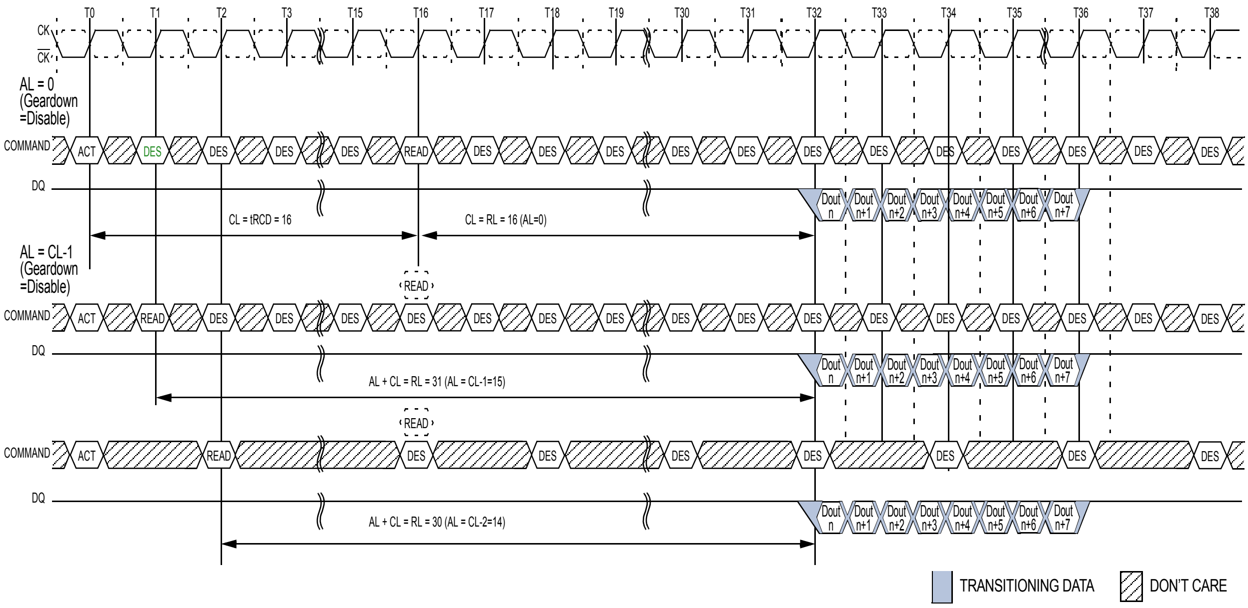
NOTE
1. Only DES is allowed during tSYNC_GEAR

Figure 51. Gear down (2N) mode entry sequence during initialization



NOTE :
1. CKE High Assert to Gear Down Enable Time (tXS, tXS_Abort) depend on MR setting.
   A correspondence of tXS/tXS_Abort and MR Setting is as follows.
   - MR4[A9] = 0 : tXS
   - MR4[A9] = 1 : tXS_Abort
2 Command not requiring locked DLL
3 Only DES is allowed during tSYNC_GEAR

Figure 52. Gear down (2N) mode entry sequence after self refresh exit (SRX)

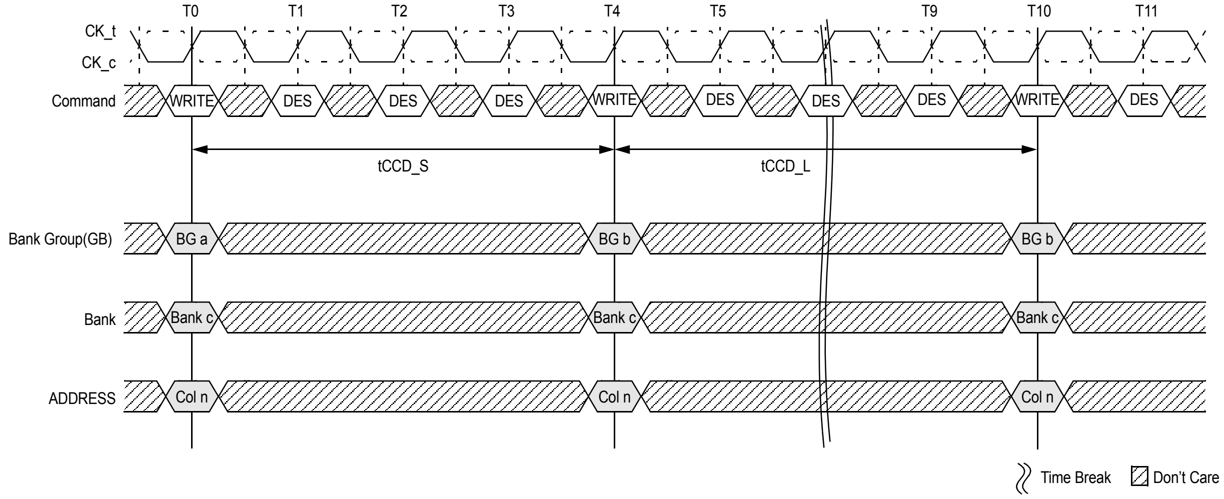


NOTE :
1. BL=8, tRCD=CL=16
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 53. Comparison Timing Diagram Between Geardown Disable and Enable.

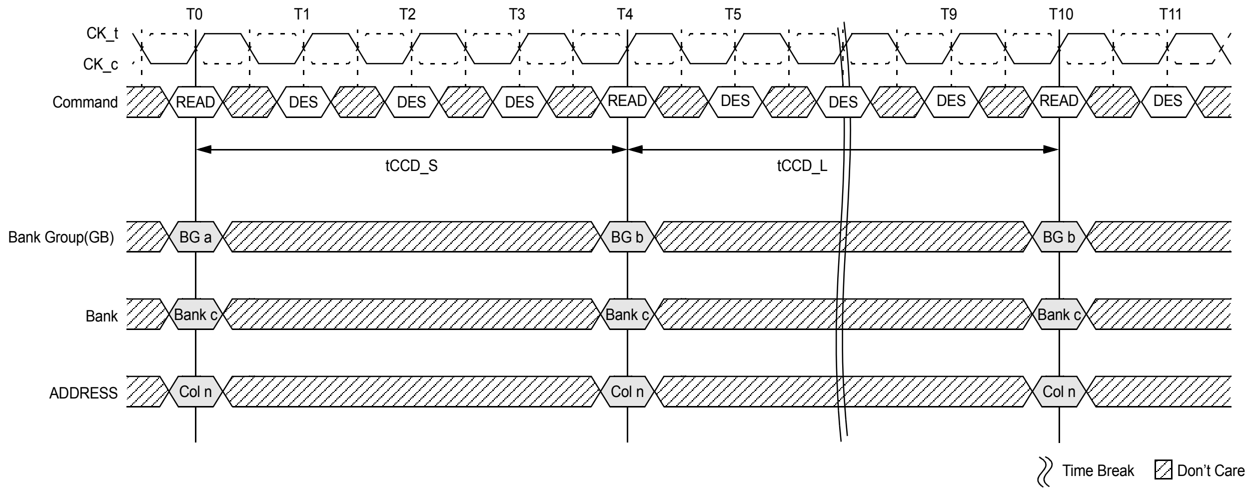
2.19 DDR4 Key Core Timing

DDR4, Core Timing



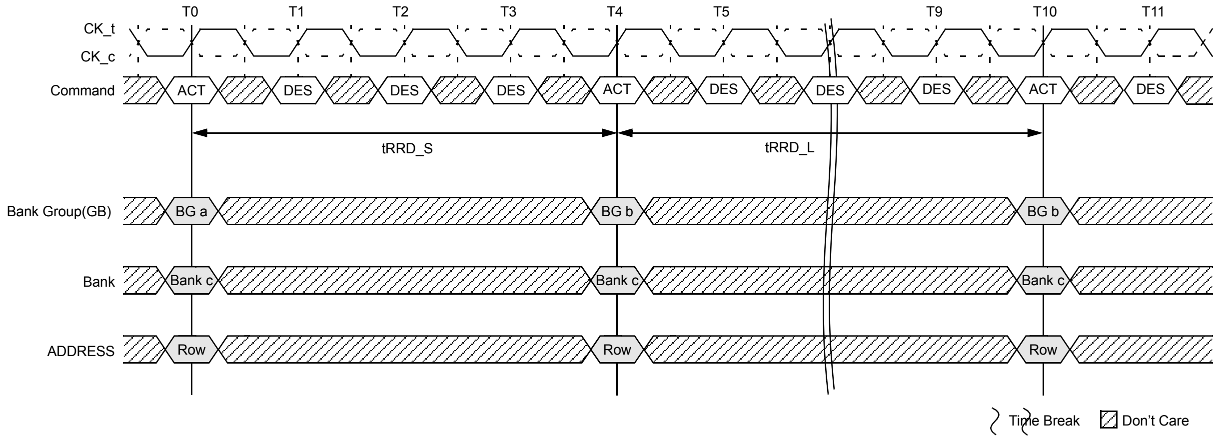
NOTE :
1. tCCD_S : CAS_n-to-CAS_n delay (short) : Applies to consecutive CAS_n to different Bank Group (i.e. T0 to T4)
2. tCCD_L : CAS_n-to-CAS_n delay (long) : Applies to consecutive CAS_n to the same Bank Group (i.e. T4 to T10)

Figure 54. tCCD Timing (WRITE to WRITE Example)



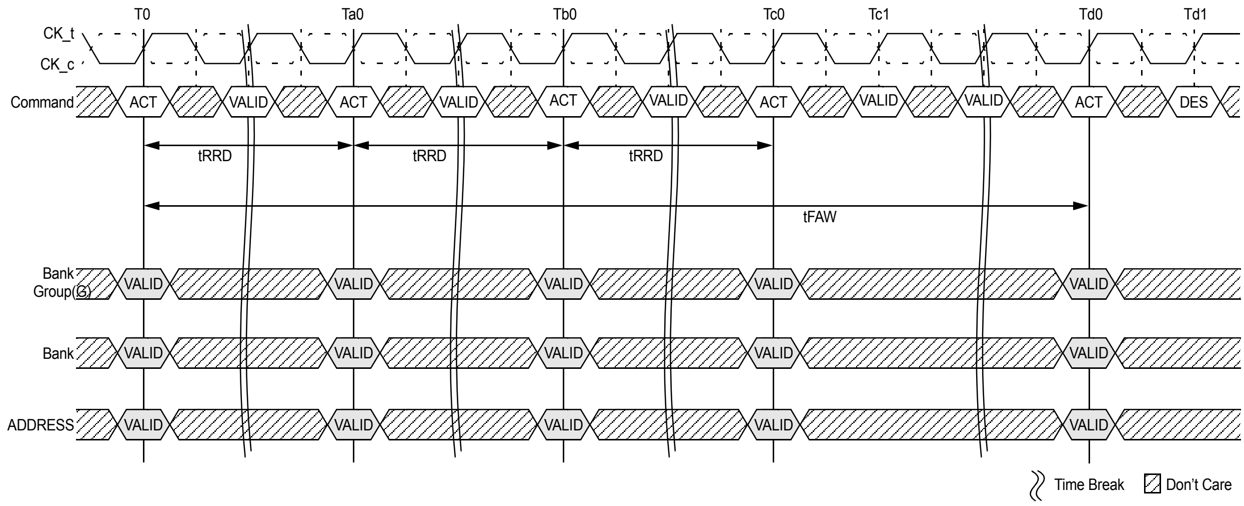
NOTE :
1. tCCD_S : CAS_n-to-CAS_n delay (short) : Applies to consecutive CAS_n to different Bank Group (i.e. T0 to T4)
2. tCCD_L : CAS_n-to-CAS_n delay (long) : Applies to consecutive CAS_n to the same Bank Group (i.e. T4 to T10)

Figure 55. tCCD Timing (READ to READ Example)



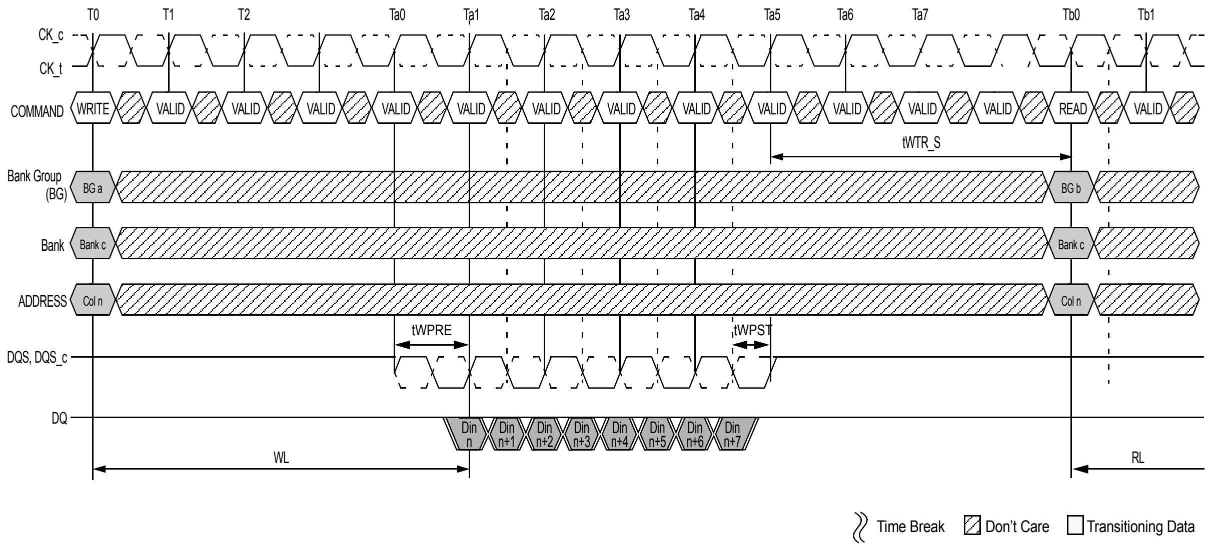
NOTE :
1. tRRD_S : ACTIVATE to ACTIVATE Command period (short) : Applies to consecutive ACTIVATE Commands to different Bank Group (i.e. T0 to T4)
2. tRRD_L : ACTIVATE to ACTIVATE Command period (long) : Applies to consecutive ACTIVATE Commands to the different Banks of the same Bank Group (i.e. T4 to T10)

Figure 56. tRRD Timing



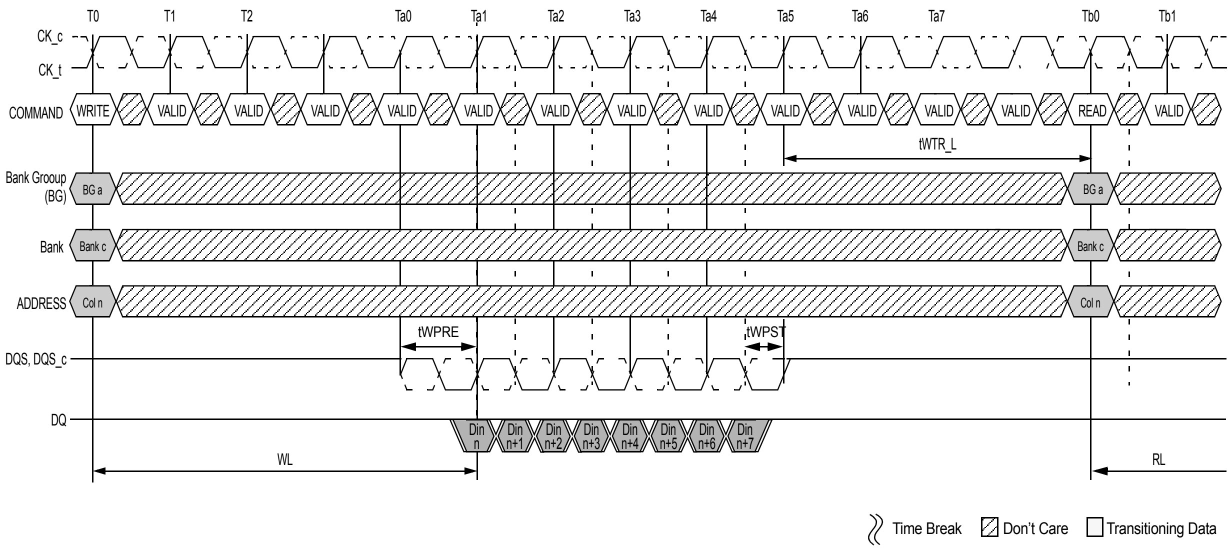
NOTE :
1. tFAW : Four activate window :

Figure 57. tFAW Timing



NOTE :
1. tWTR_S : Delay from start of internal write transaction to internal read command to a different Bank Group.

Figure 58. tWTR_S Timing (WRITE to READ, Different Bank Group, CRC and DM Disabled)



NOTE :
1. tWTR_L : Delay from start of internal write transaction to internal read command to the same Bank Group.

Figure 59. tWTR_L Timing (WRITE to READ, Same Bank Group, CRC and DM Disabled)

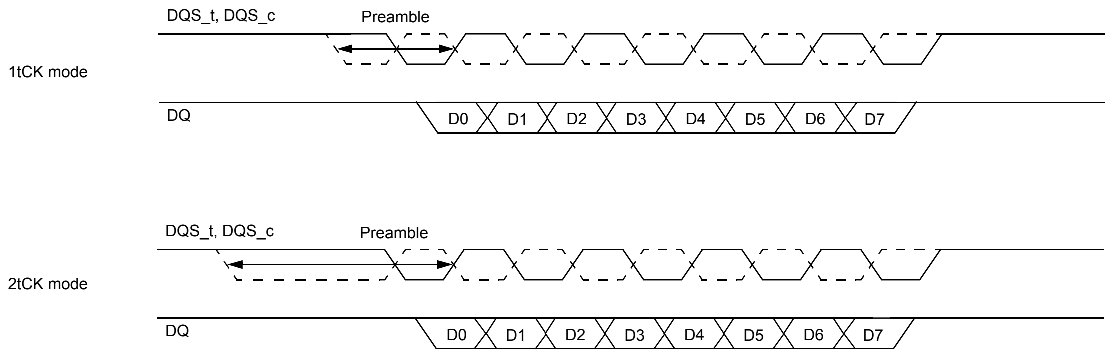
2.20 Programmable Preamble

The DQS preamble can be programmed to one or the other of 1 tCK and 2 tCK preamble ; selectable via MRS (MR4 [A12, A11]). The 1 tCK preamble applies to all speed-Grade and The 2 tCK preamble is valid for DDR4-2400/2666/3200 Speed bin Tables.

2.20.1 Write Preamble

DDR4 supports a programmable write preamble.The 1 tCK or 2tCK Write Preamble is selected via MR4 [A12].
Write preamble modes of 1 tCK and 2 tCK are shown below.

When operating in 2 tCK Write preamble mode ; in MR2 Table-6, CWL of 1st Set needs to be incremented by 2 nCK and CWL of 2nd Set does not need increment of it. tWTR and tWR must be programmed to a value one or two clock, depending on available settings, greater than the tWTR and tWR setting required in the applicable speed bin table.



The timing diagrams contained in Figure 60, Figure 61 and Figure 62 illustrate 1 and 2 tCK preamble scenarios for consecutive write commands with tCCD timing of 4, 5 and 6 nCK, respectively. Setting tCCD to 5nCK is not allowed in 2 tCK preamble mode

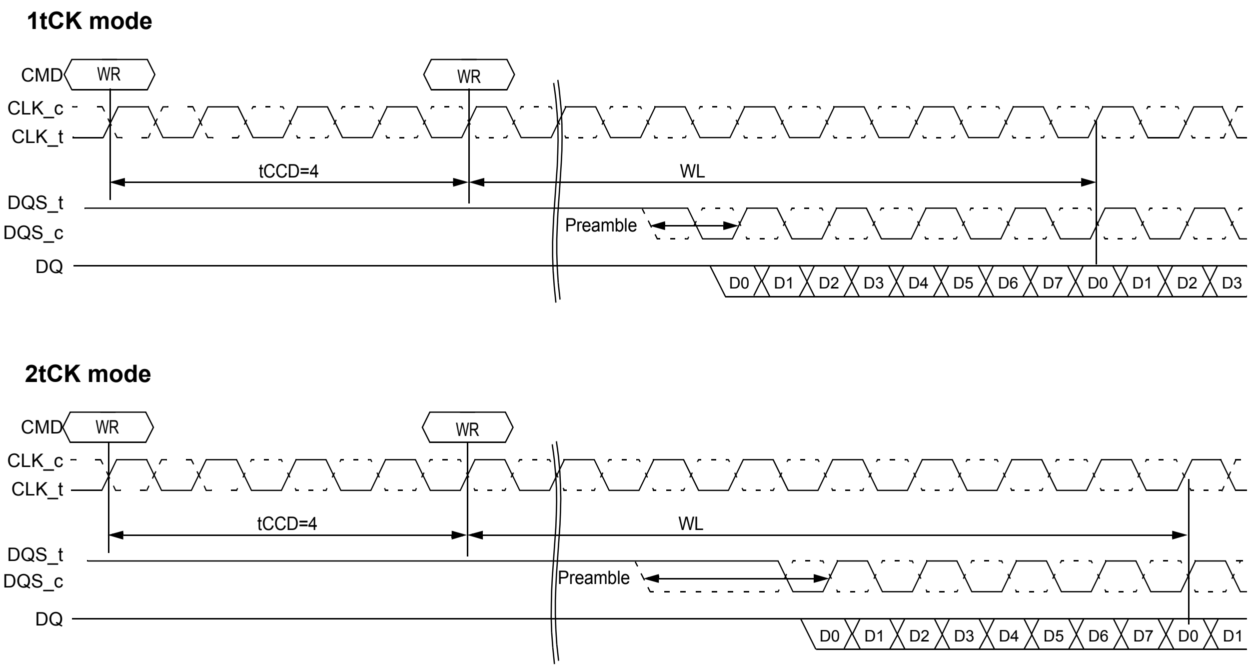
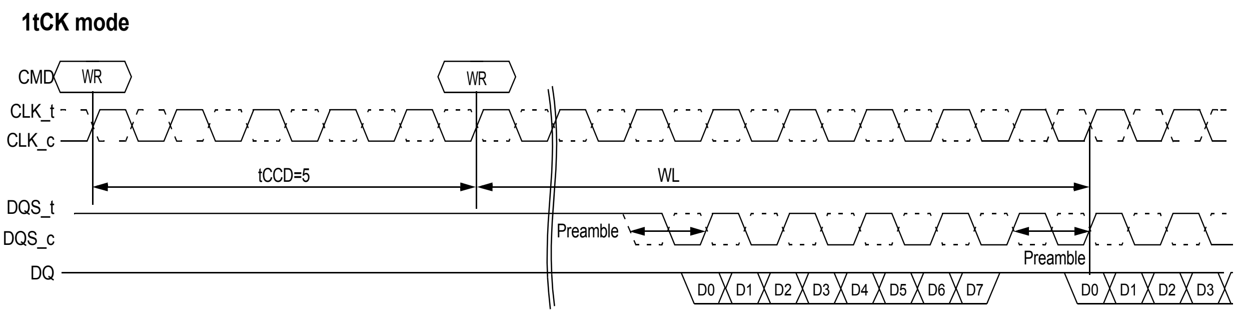


Figure 60. tCCD=4 (AL=PL=0)



2tCK mode: tCCD=5 is not allowed in 2tCK mode

Figure 61. tCCD=5 (AL=PL=0)

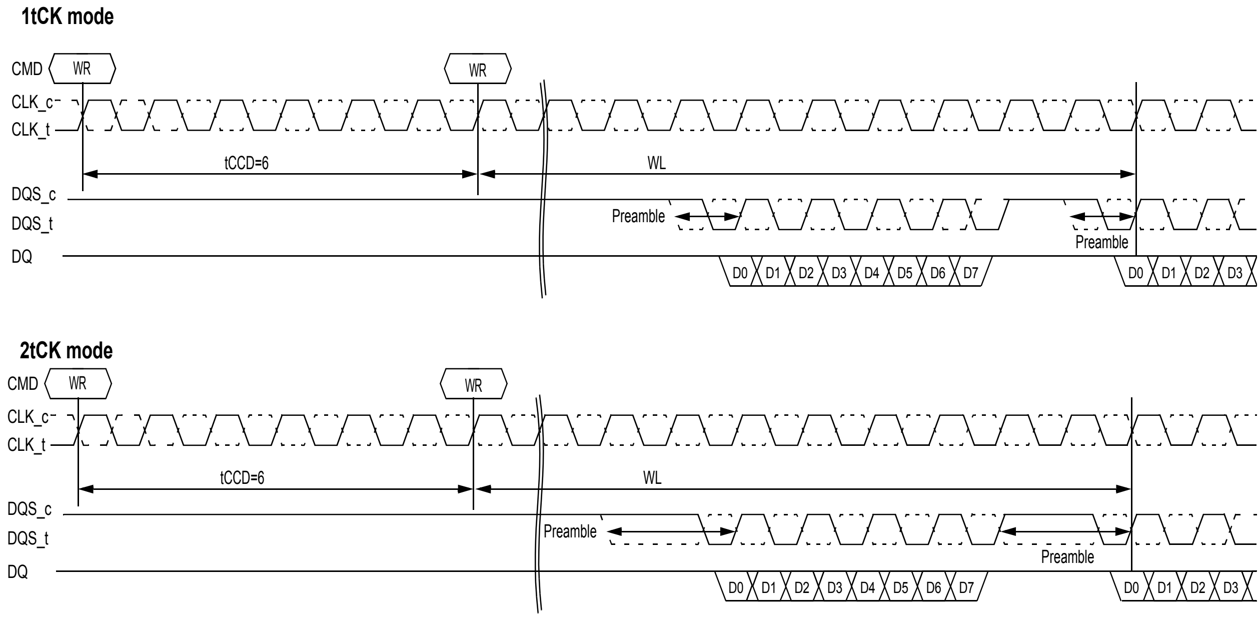
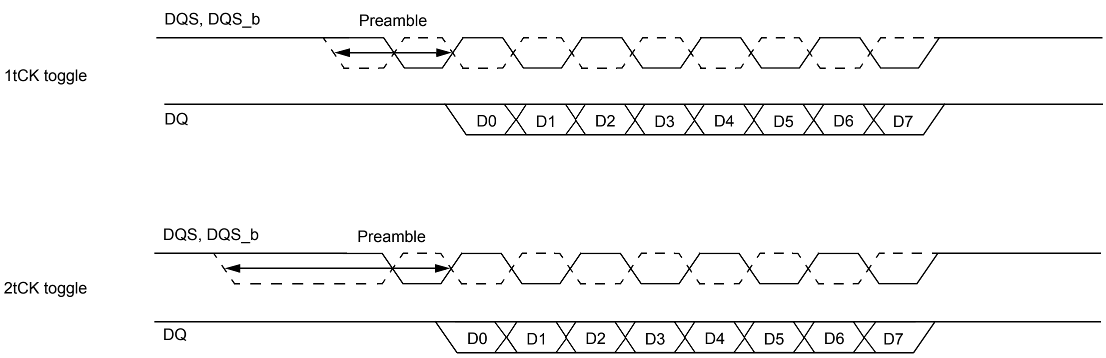


Figure 62. tCCD=6 (AL=PL=0)

2.20.2 Read Preamble

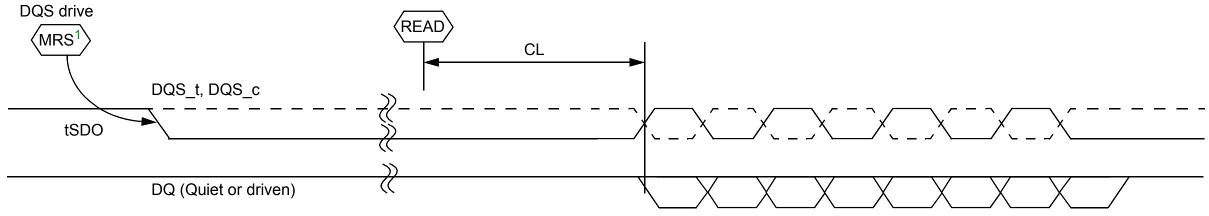
DDR4 supports a programmable read preamble. The 1 tCK and 2 tCK Read preamble is selected via MR4 [A11]. Read preamble modes of 1 tCK and 2 tCK are shown below.



2.20.3 Read Preamble Training

Read Preamble Training, shown below, can be enabled via MR4 [A10] when the DRAM is in the MPR mode. Read Preamble Training is illegal if DRAM is not in the MPR mode. The Read Preamble Training can be used for read leveling.

Illegal READ commands, any command during the READ process or initiating the READS process, are not allowed during Read Preamble Training.



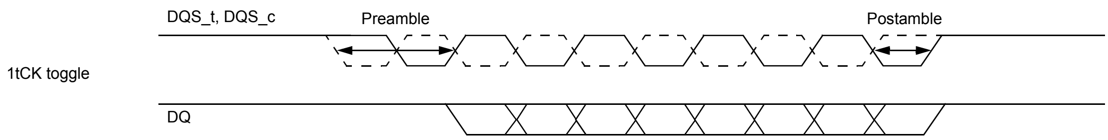
NOTE
1. Read Preamble Training mode is enabled by MR4 A10 = [1]

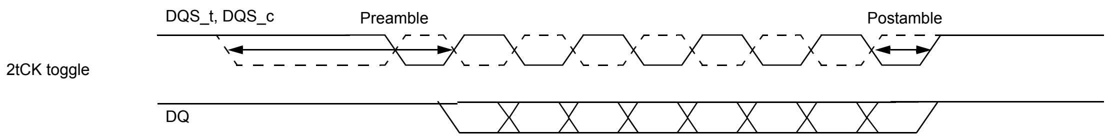
Parameter	Symbol	DDR4-1600,1866,2133,2400		DDR4-2666,3200		Units	NOTE
		Min	Max	Min	Max		
Delay from MRS Command to Data Strobe Drive Out	tSDO	-	tMOD+9ns	-	tMOD+9ns		

2.21 Postamble

2.21.1 Read Postamble

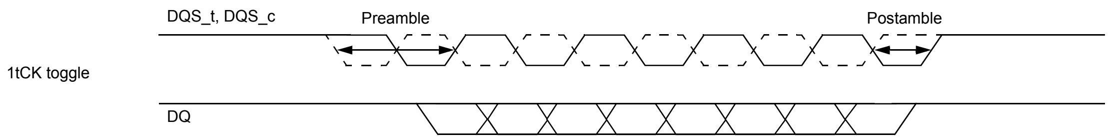
DDR4 will support a fixed read postamble.
Read postamble of nominal 0.5tck for preamble modes 1,2 Tck are shown below:

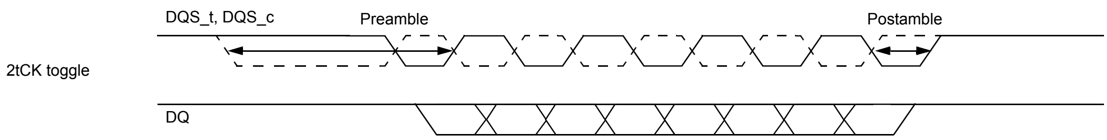




2.21.2 Write Postamble

DDR4 will support a fixed Write postamble.
Write postamble nominal is 0.5tck for preamble modes 1,2 Tck are shown below:





2.22 ACTIVATE Command

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG0-BG1 in X4/8 and BG0 in X16 select the bankgroup; BA0-BA1 inputs selects the bank within the bankgroup, and the address provided on inputs A0-A17 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

2.23 Precharge Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

If A10 is High when Read or Write command is issued, then auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read. Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array. The bank will be avaiable for a subsequent row activation a specified time (tRP) after hidden PRECHARGE command (AutoPrecharge) is issued to that bank.

2.24 Read Operation

2.24.1 READ Timing Definitions

Read timing shown in this section is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK_t, CK_c.
- tDQSCK is the actual position of a rising strobe edge relative to CK_t, CK_c.
- tQSH describes the DQS_t, DQS_c differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS_t, DQS_c differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.

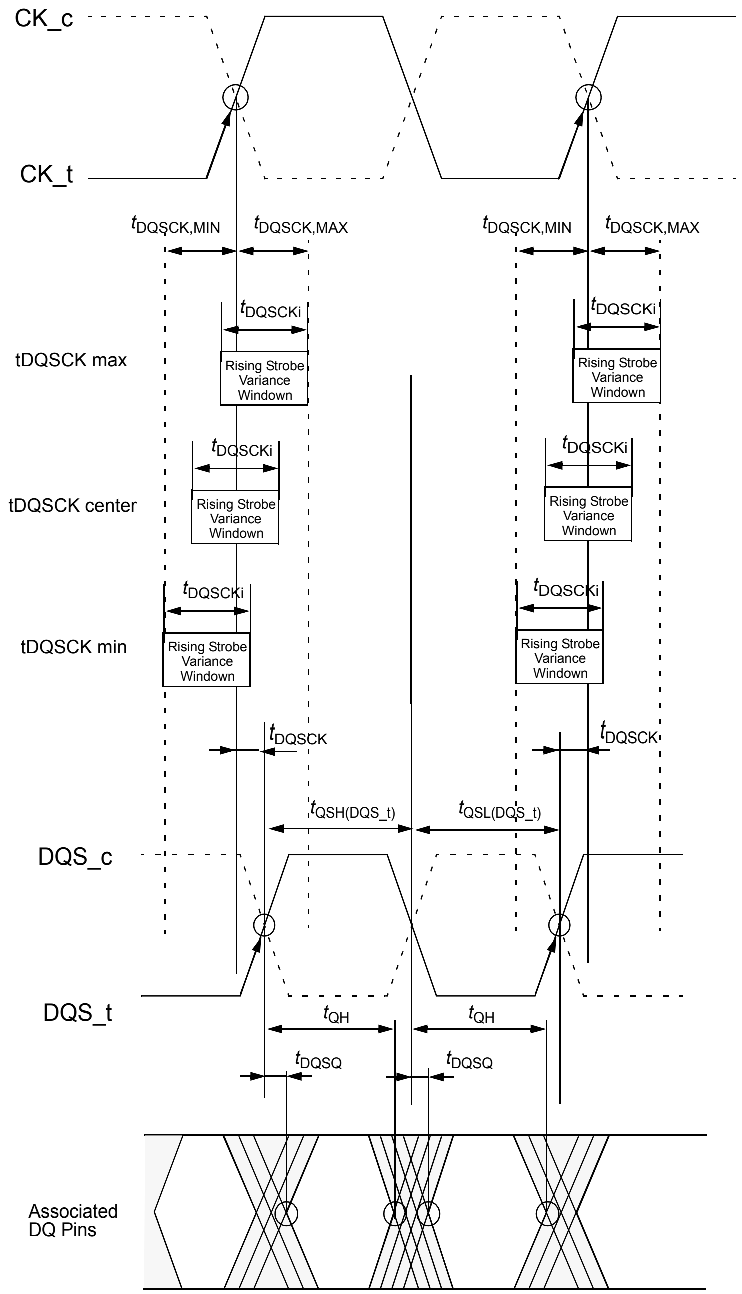


Figure 63. READ Timing Definition

[Table 53] **Data Output Timing**

Parameter	Symbol	DDR4-1600,1866 Min	DDR4-1600,1866 Max	DDR4-2133 Min	DDR4-2133 Max	DDR4-2400 Min	DDR4-2400 Max	Units	NOTE
Data Timing									
DQS_t,DQS_c to DQ Skew per group, per access	tDQSQ	-	0.16	-	0.16		0.17	UI	1,4
DQ output hold time from DQS_t, DQS_c	tQH	0.76	-	0.76	-	0.74		UI	1,3,4
Data Valid Window per device: tQH-tDQSQ for a device at same voltage and temperature	tDVWd	0.63		0.64		0.64		UI	2,3,4
Data Valid Window per pin: tQH-tDQSQ each device output at same voltage and temperature	tDVWp	0.66		0.69		0.72		UI	2,3,4
Data Strobe Timing									
DQS, DQS# differential output low time	tQSL	0.4		0.4		0.4		UI	5
DQS, DQS# differential output high time	tQSH	0.4		0.4		0.4		UI	6

Unit UI = tCK(avg).min/2

NOTE:

1. DQ to DQS timing per group
2. This parameter will be characterized and guaranteed by design.
3. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
4. DRAM DBI mode is off.
5. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
6. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on rising edge to the next consecutive falling edge

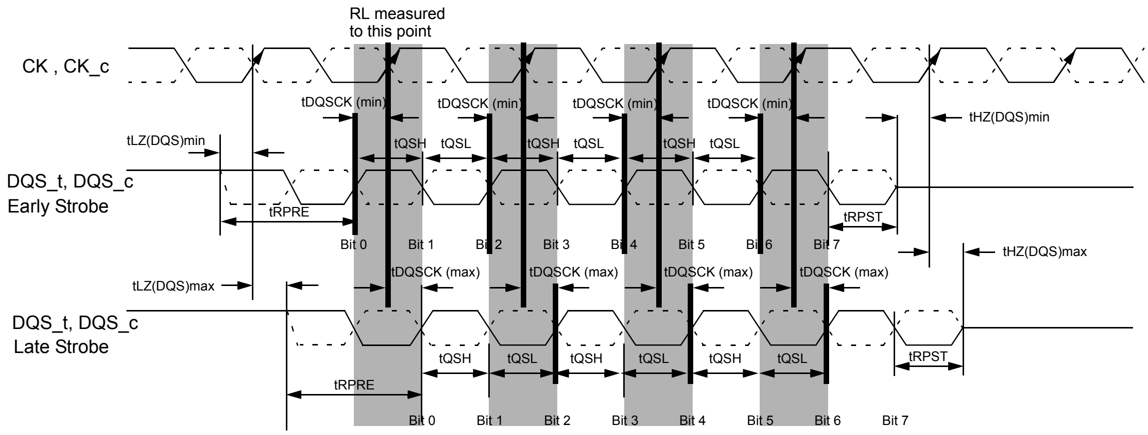
2.24.1.1 READ Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in Figure 64 and is applied when the DLL is enabled and locked.
Rising data strobe edge parameters:

- •tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK_t, CK_c.
- •tDQSCK is the actual position of a rising strobe edge relative to CK_t, CK_c.
- •tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.
- tLZ(DQS), tHZ(DQS) for preamble/postamble.



NOTE :

1. Within a burst, rising strobe edge can be varied within tDQSCKi while at the same voltage and temperature. However incorporate the device, voltage and temperature variation, rising strobe edge variance window, can shift between tDQSCK(min) and tDQSCK(max). A timing of this window's right inside edge (latest) from rising CK_t, CK_c is limited by a device's actual tDQSCK(max). A timing of this window's left inside edge (earliest) from rising CK_t, CK_c is limited by tDQSCK(min).

2. Notwithstanding note 1, a rising strobe edge with tDQSCK(max) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK(min) at T(n+1). This is because other timing relationships (tQSH, tQSL) exist:
   if tDQSCK(n+1) < 0:
   tDQSCK(n) < 1.0 tCK - (tQSHmin + tQSLmin) - |tDQSCK(n+1)|
3. The DQS_t, DQS_c differential output high time is defined by tQSH and the DQS_t, DQS_c differential output low time is defined by tQSL.
4. Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCKmin (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCKmax (late strobe case).
5. The minimum pulse width of read preamble is defined by tRPRE(min).
6. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZDQS(max) on the right side.
7. The minimum pulse width of read postamble is defined by tRPST(min).
8. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.

Figure 64. Clock to Data Strobe Relationship

2.24.1.2 READ Timing; Data Strobe to Data relationship

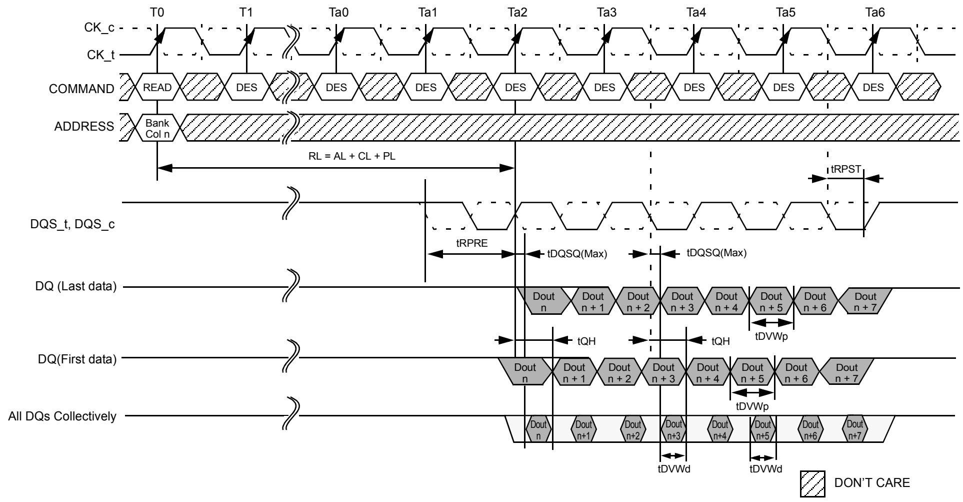
The Data Strobe to Data relationship is shown in Figure 65 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.

Data Valid Window:
- tDVWd is the Data Valid Window per device and is derived from the smallest (earliest) observable tQH minus the largest (slowest) observable tDQSQ on a given DRAM.
- tDVWp is Data Valid Window per pin per device and is derived by determining the tDVWd component for each of the device's data output.

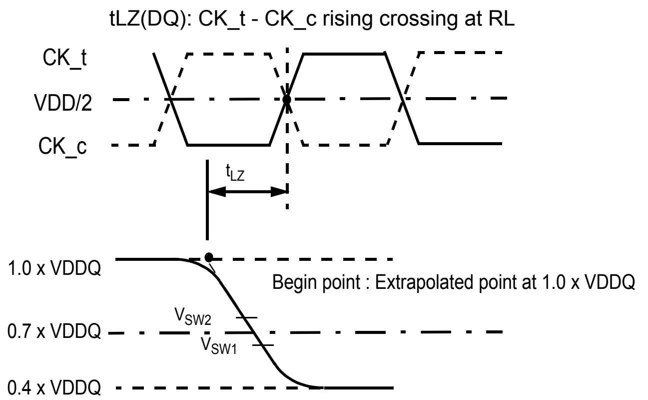


NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
5. Output timings are referenced to VDDQ, and DLL on for locking.
6. tDQSQ defines the skew between DQS_t,DQS_c to Data and does not define DQS_t, DQS_c to Clock.
7.Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst

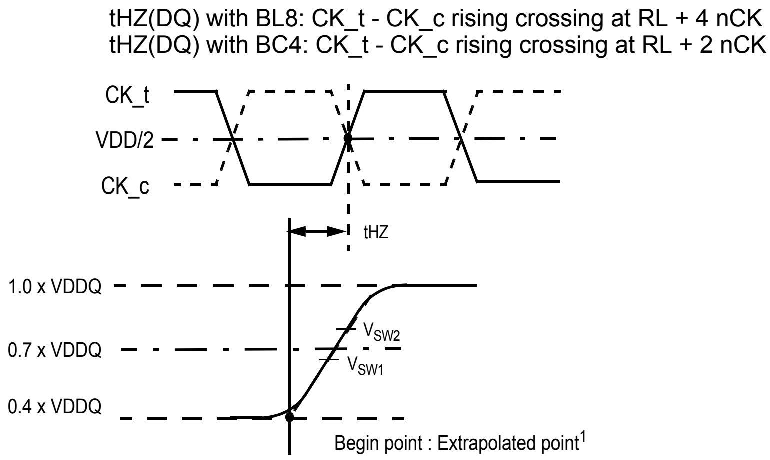
Figure 65. Data Strobe to Data Relationship

2.24.1.3 tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ).
Figure 66 shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single ended.



tLZ(DQ) begin point is above-mentioned extrapolated point.



tHZ(DQ) is begin point is above-mentioned extrapolated point.

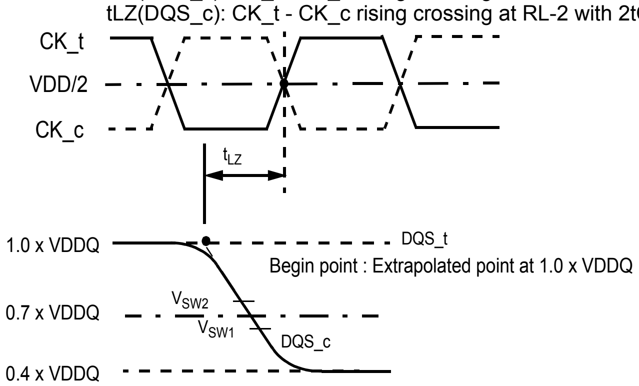
NOTE 1 Extrapolated point (Low Level) = VDDQ/(50+34) X 34
= VDDQ x 0.40
- A driver impedance : RZQ/7(34ohm)
- An effective test load : 50 ohm to VTT = VDDQ

Figure 66. tLZ(DQ) and tHZ(DQ) method for calculating transitions and begin points

[Table 54] Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements

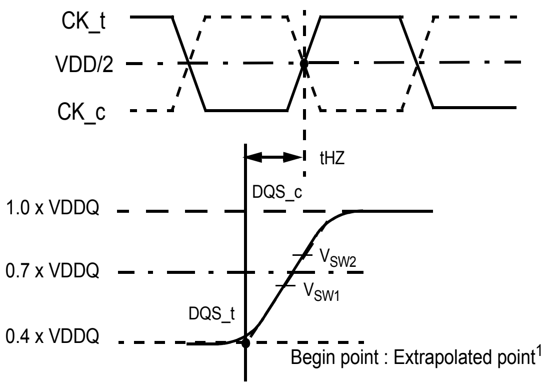
Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	(0.70 - 0.04) x VDDQ	(0.70 + 0.04) x VDDQ	
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	(0.70 - 0.04) x VDDQ	(0.70 + 0.04) x VDDQ	

tLZ(DQS_c): CK_t - CK_c rising crossing at RL-1 with 1tCK Preamble
tLZ(DQS_c): CK_t - CK_c rising crossing at RL-2 with 2tCK Preamble



tLZ(DQS_c) begin point is above-mentioned extrapolated point.

tHZ(DQS_t) with BL8: CK_t - CK_c rising crossing at RL + 4 nCK
tHZ(DQS_t) with BC4: CK_t - CK_c rising crossing at RL + 2 nCK



tHZ(DQS_t) begin point is above-mentioned extrapolated point.

NOTE 1 Extrapolated point (Low Level) = VDDQ/(50+34) X 34
= VDDQ x 0.40
- A driver impedance : RZQ/7(34ohm)
- An effective test load : 50 ohm to VTT = VDDQ

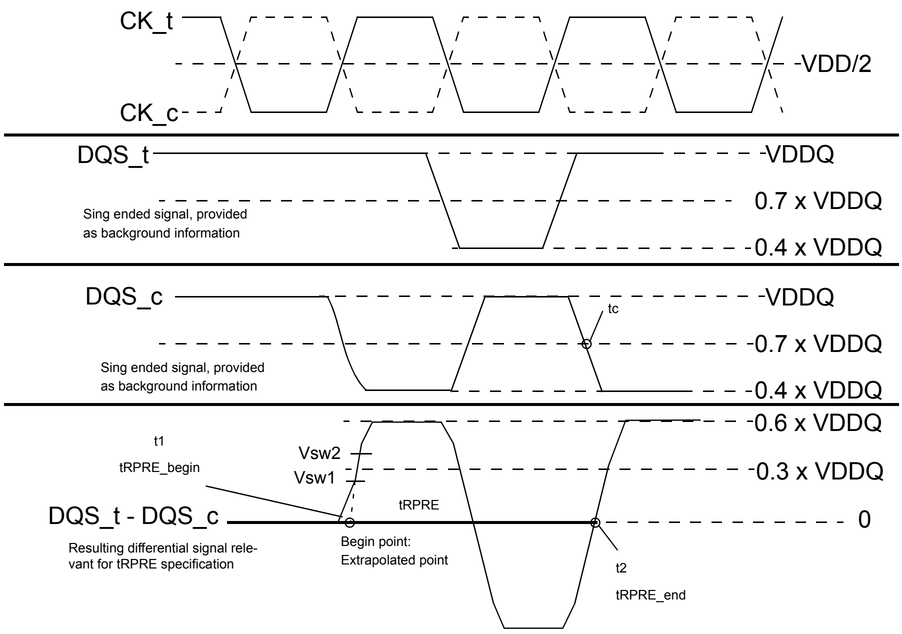
Figure 67. tLZ(DQS_c) and tHZ(DQS_t) method for calculating transitions and begin points

[Table 55] Reference Voltage for tLZ(DQS_c), tHZ(DQS_t) Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQS_c low-impedance time from CK_t, CK_c	tLZ(DQS_c)	(0.70 - 0.04) x VDDQ	(0.70 + 0.04) x VDDQ	
DQS_t high impedance time from CK_t, CK_c	tHZ(DQS_t)	(0.70 - 0.04) x VDDQ	(0.70 + 0.04) x VDDQ	

2.24.1.4 tRPRE Calculation

The method for calculating differential pulse widths for tRPRE is shown in Figure 68.



NOTE:

1. Low Level of DQS_t and DQS_c = VDDQ/(50+34) x 34
   = VDDQ x 0.40
   - A driver impedance : RZQ/7(34ohm)
   - An effective test load : 50 ohm to VTT = VDDQ

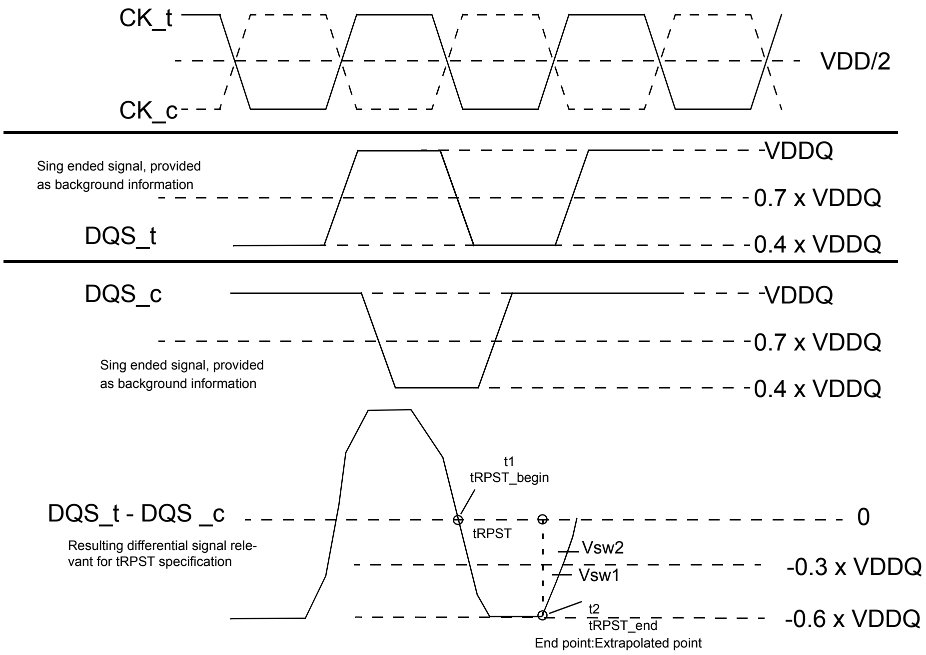
Figure 68. Method for calculating tRPRE transitions and endpoints

[Table 56] Reference Voltage for tRPRE Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQS_t, DQS_c differential READ Preamble	tRPRE	(0.30 - 0.04) x VDDQ	(0.30 + 0.04) x VDDQ	

2.24.1.5 tRPST Calculation

The method for calculating differential pulse widths for tRPST is shown in Figure 69.



NOTE:

1. Low Level of DQS_T and DQS_c = VDDQ/(50+34) x 34
   = VDDQ x 0.40
   - A driver impedance : RZQ/7(34ohm)
   - An effective test load : 50 ohm to VTT = VDDQ

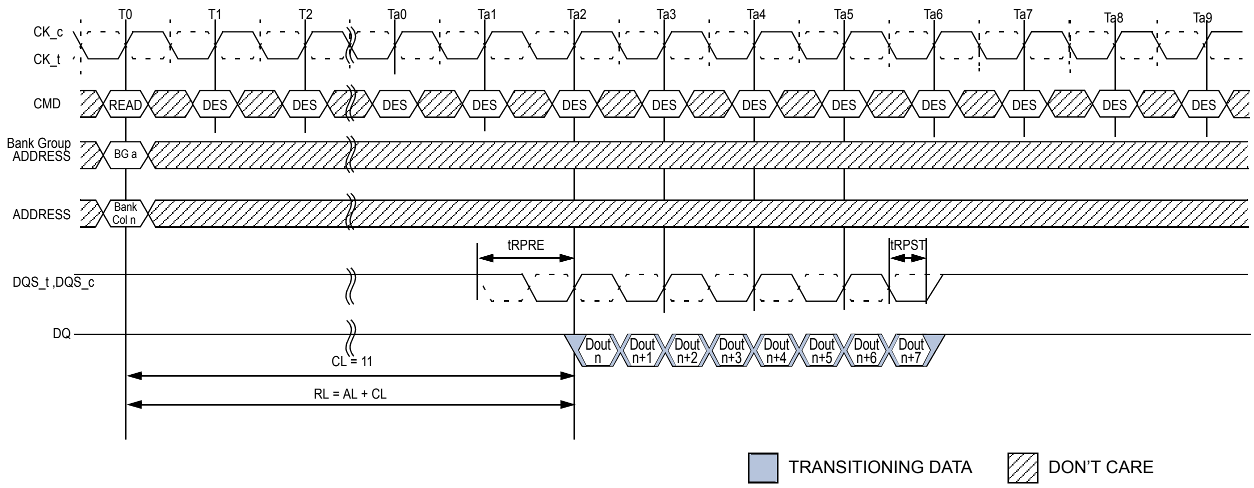
Figure 69. Method for calculating tRPST transitions and endpoints

[Table 57] Reference Voltage for tRPST Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQS_t, DQS_c differential READ Postamble	tRPST	(-0.30 - 0.04) x VDDQ	(-0.30 + 0.04) x VDDQ	

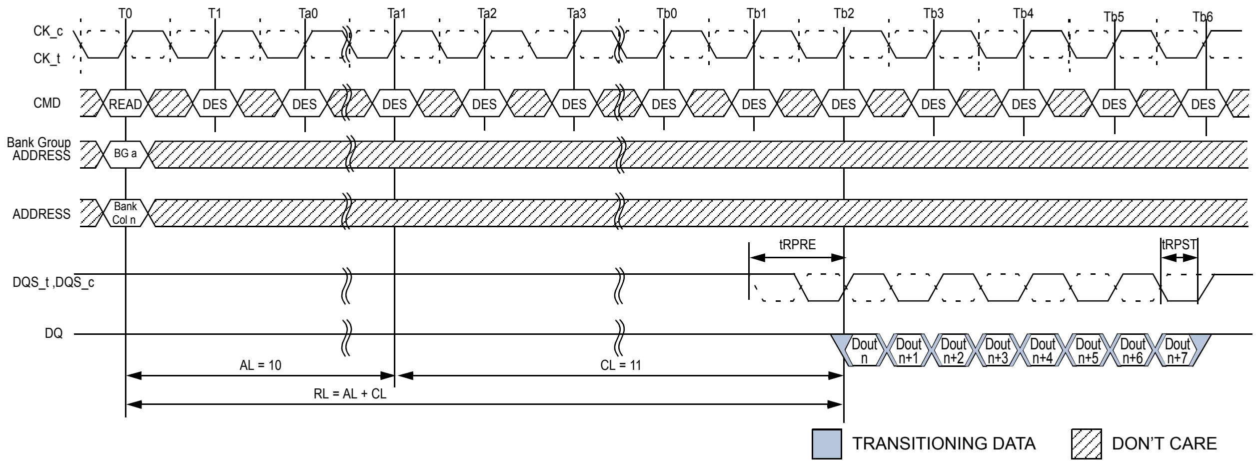
2.24.2 READ Burst Operation

During a READ or WRITE command, DDR4 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).
A12 = 0 : BC4 (BC4 = burst chop)
A12 = 1 : BL8
A12 is used only for burst length control, not as a column address.



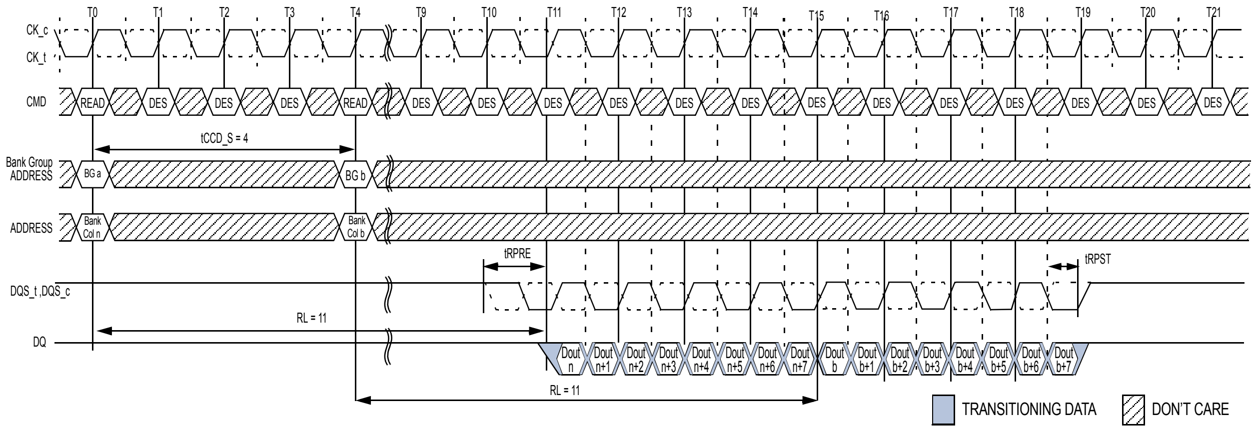
NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 70. READ Burst Operation RL = 11 (AL = 0, CL = 11, BL8)



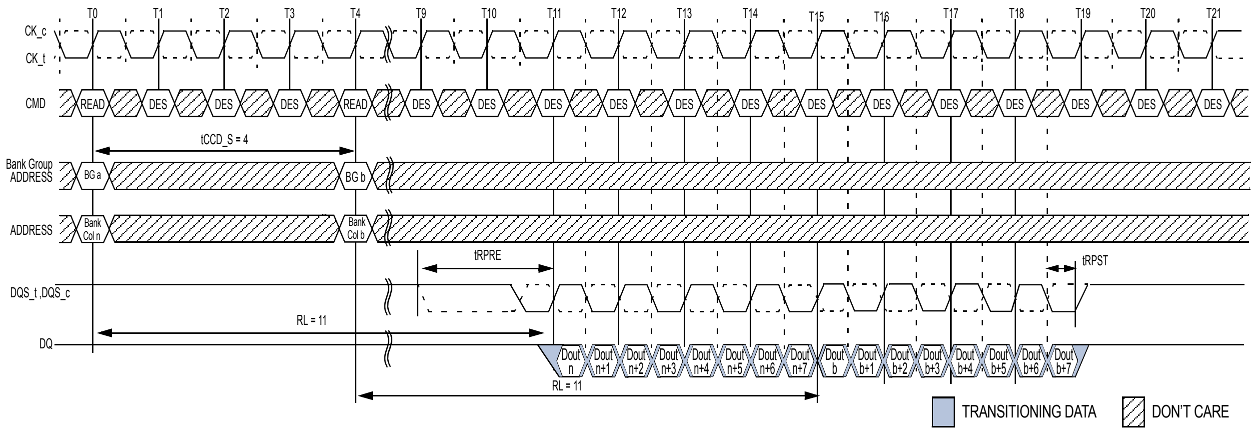
NOTE :
1. BL = 8, RL = 21, AL = (CL-1), CL = 11, Preamble = 1tCK
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 71. READ Burst Operation RL = 21 (AL = 10, CL = 11, BL8)



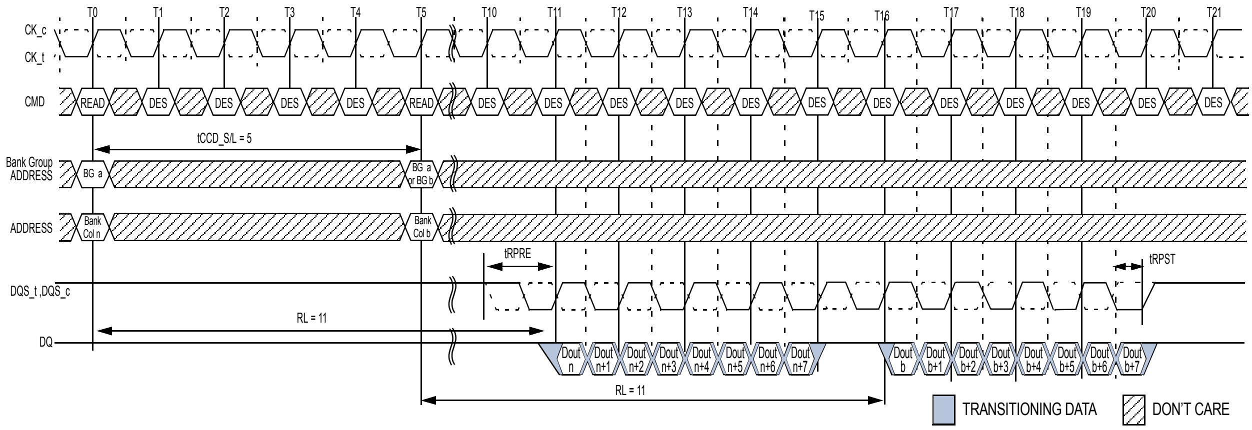
NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 72. Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group



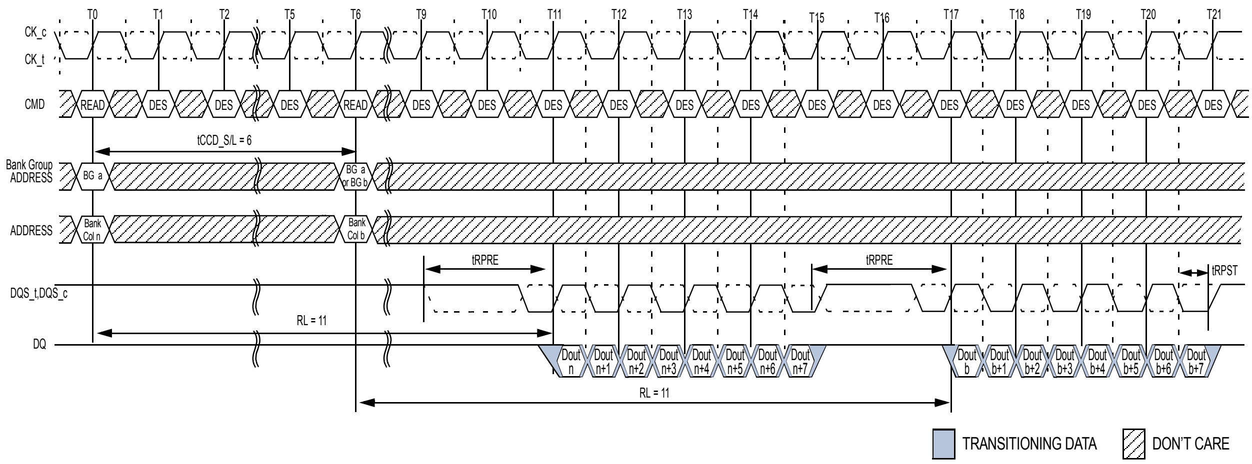
NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A:0 = 0:1] and A12 = 1 during READ command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 73. Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group



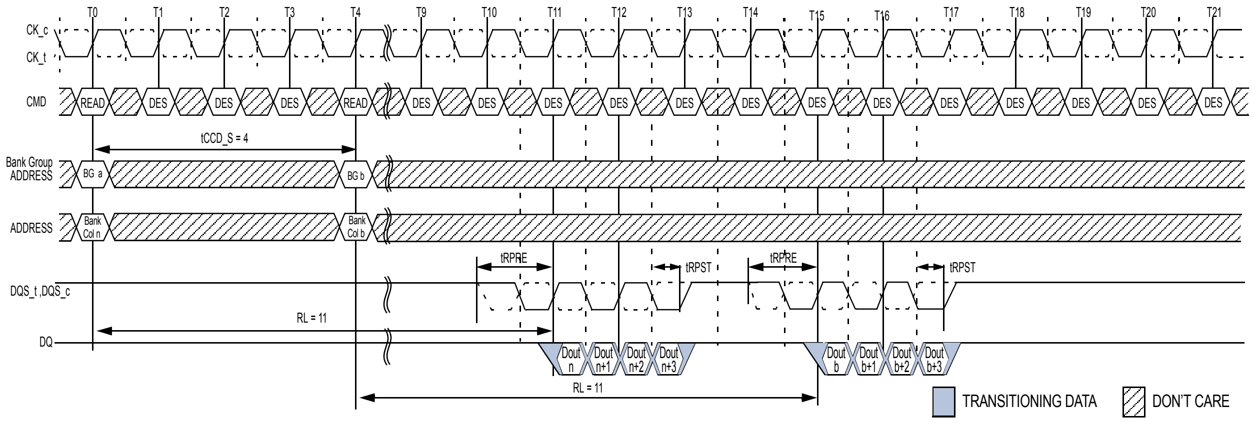
NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tCCD_S/L = 5
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T5.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 74. Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group



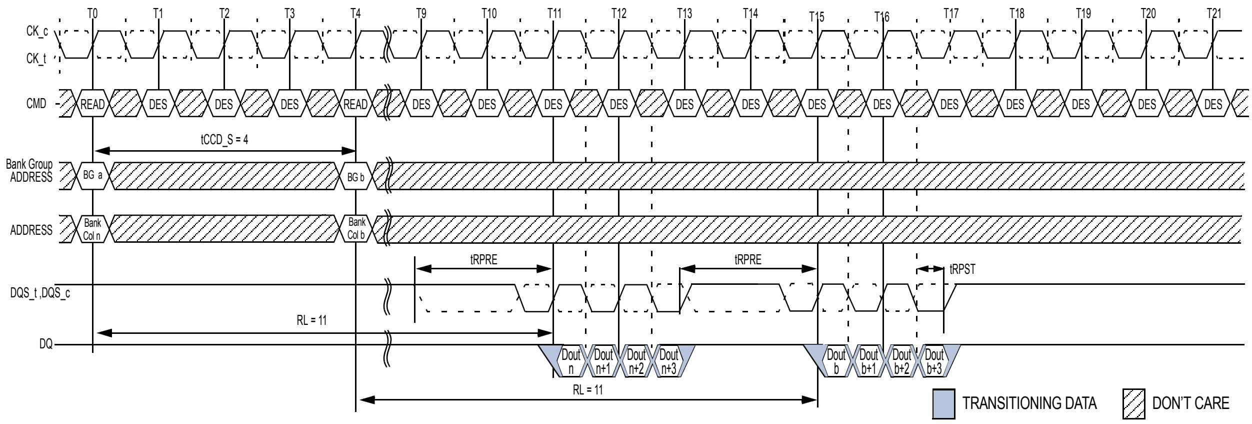
NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 2tCK, tCCD_S/L = 6
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable
6. tCCD_S/L=5 isn't allowed in 2tCK preamble mode.

Figure 75. Nonconsecutive READ (BL8) with 2tCK Preamble in Same or Different Bank Group



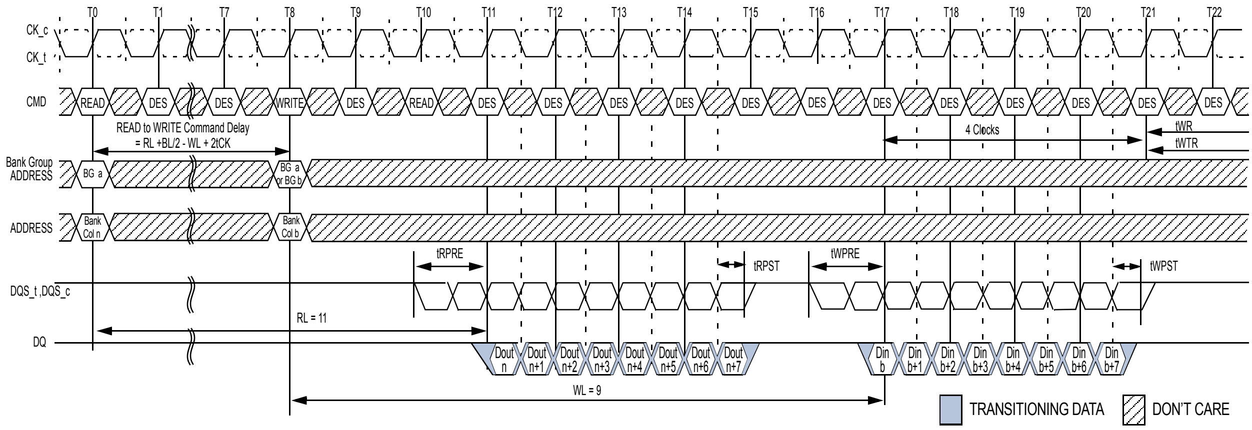
NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 76. READ (BC4) to READ (BC4) with 1tCK Preamble in Different Bank Group



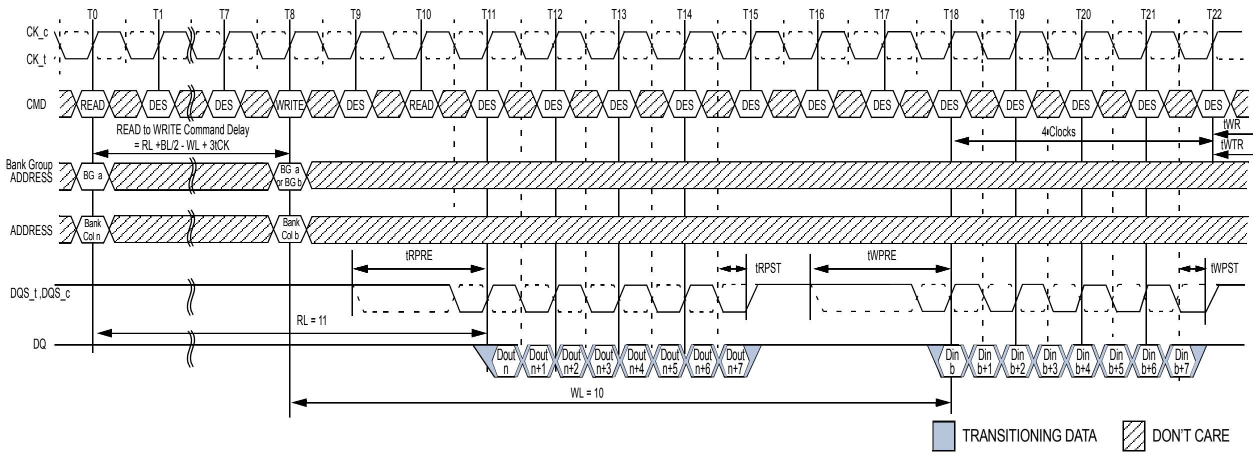
NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 77. READ (BC4) to READ (BC4) with 2tCK Preamble in Different Bank Group



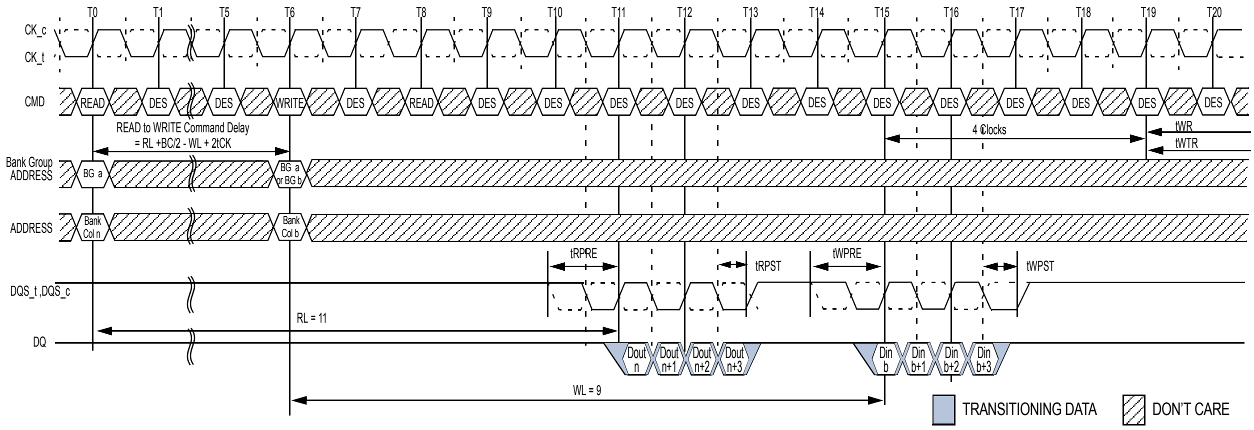
NOTE :
1. BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 78. READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



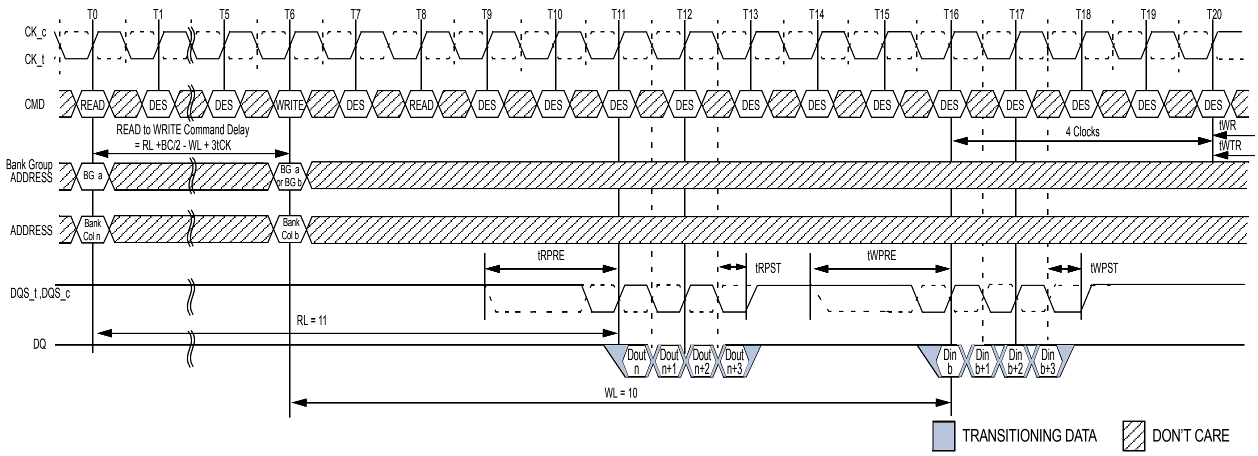
NOTE :
1. BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 79. READ (BL8) to WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



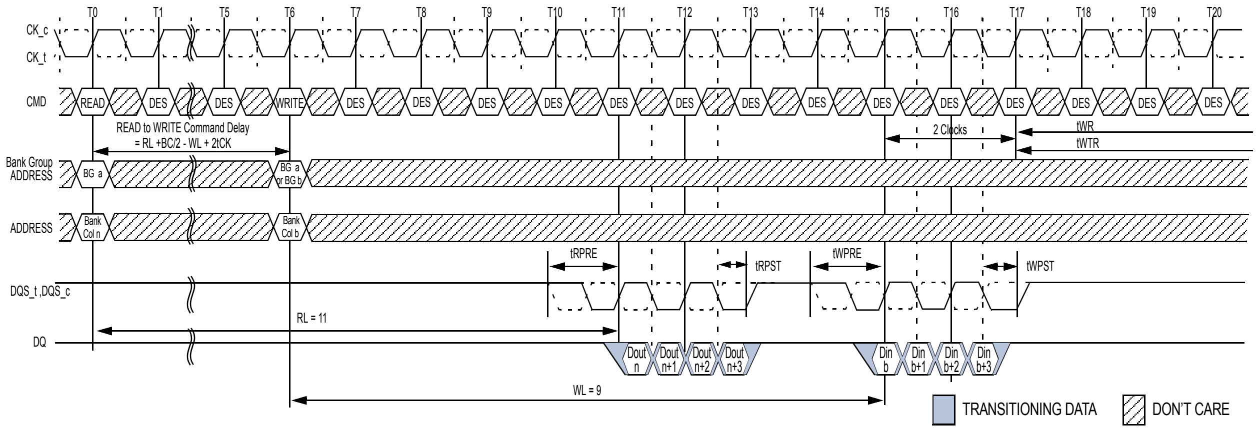
NOTE :
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 80. READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



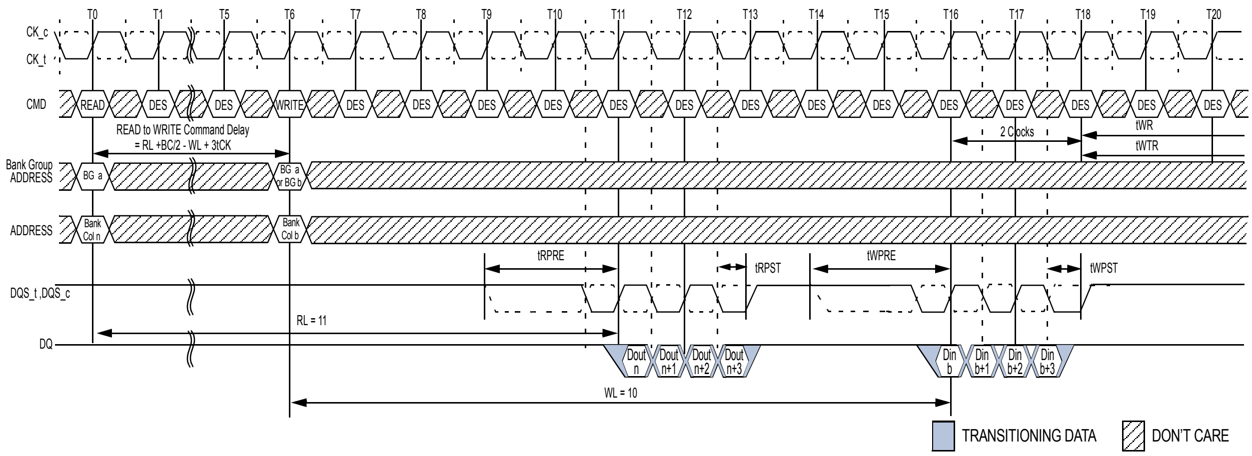
NOTE :
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 81. READ (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



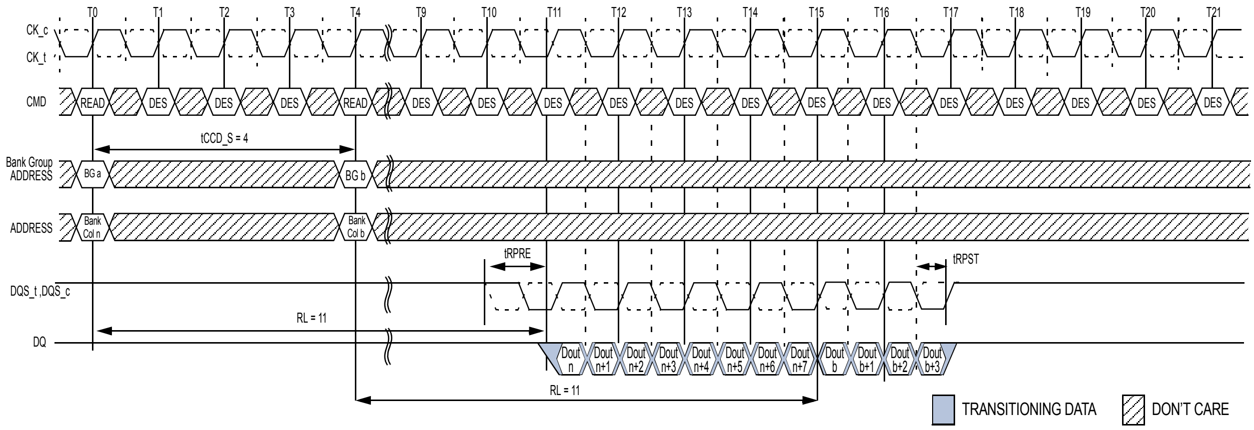
NOTE :
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(Fixed) setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 82. READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Same or Different Bank Group



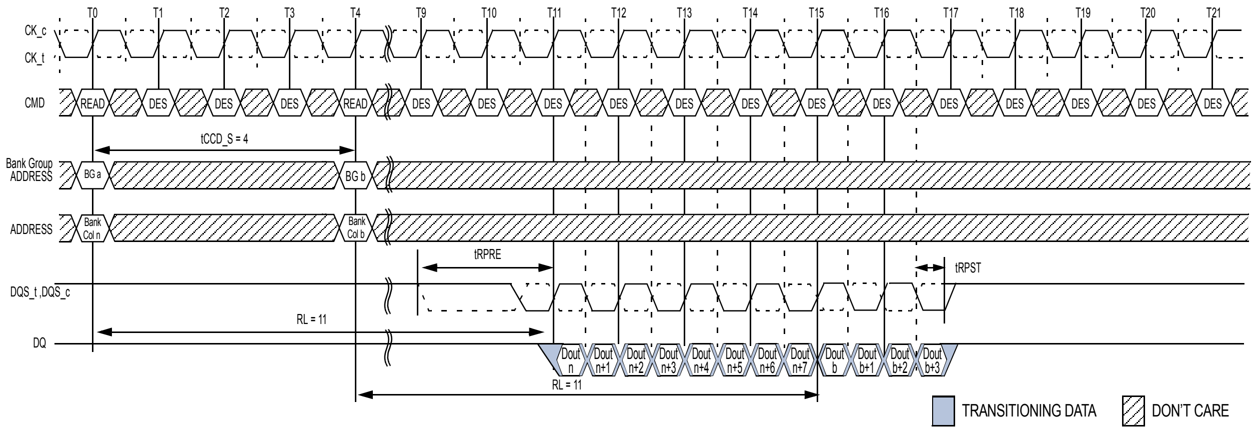
NOTE :
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(Fixed) setting activated by MR0[A1:A0 = 1:0].
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 83. READ (BC4) Fixed to WRITE (BC4) Fixed with 2tCK Preamble in Same or Different Bank Group



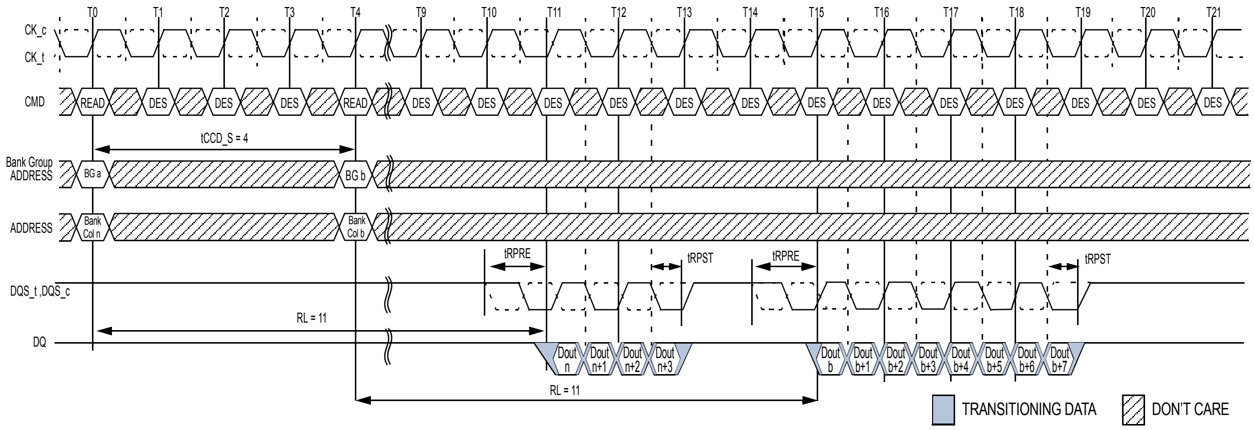
NOTE :
1. BL = 8, AL =0, CL = 11 ,Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 84. READ (BL8) to READ (BC4) OTF with 1tCK Preamble in Different Bank Group



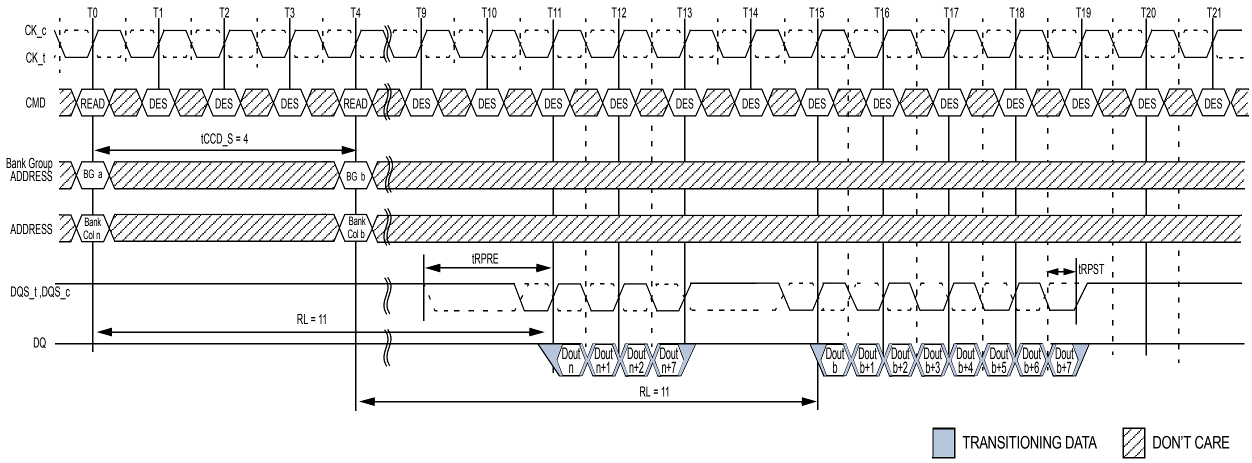
NOTE :
1. BL = 8, AL =0, CL = 11 ,Preamble = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 85. READ (BL8) to READ (BC4) OTF with 2tCK Preamble in Different Bank Group



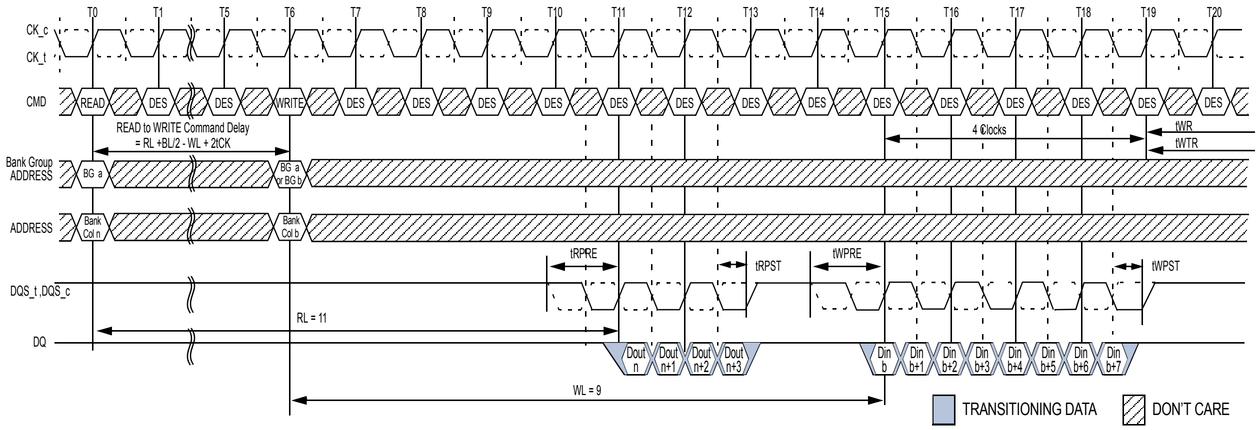
NOTE :
1. BL = 8, AL =0, CL = 11 ,Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 86. READ (BC4) to READ (BL8) OTF with 1tCK Preamble in Different Bank Group



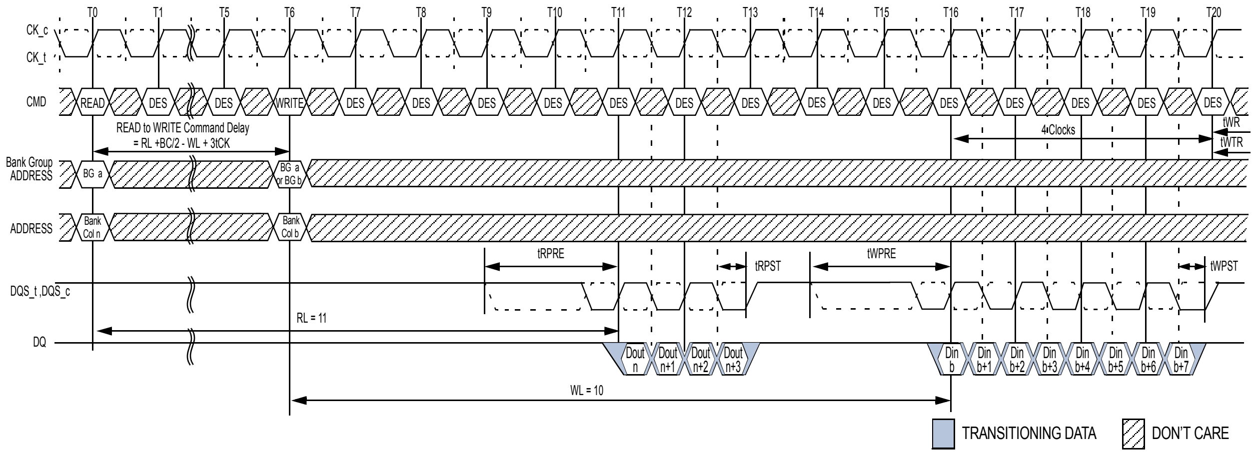
NOTE :
1. BL = 8, AL =0, CL = 11 ,Preamble = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 87. READ (BC4) to READ (BL8) OTF with 2tCK Preamble in Different Bank Group



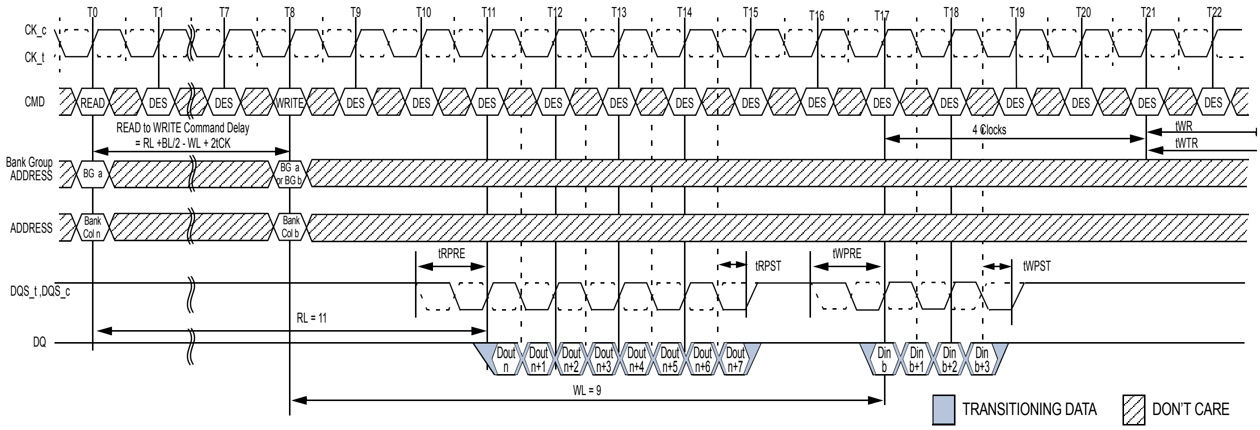
NOTE :
1. BC = 4, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 88. READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group



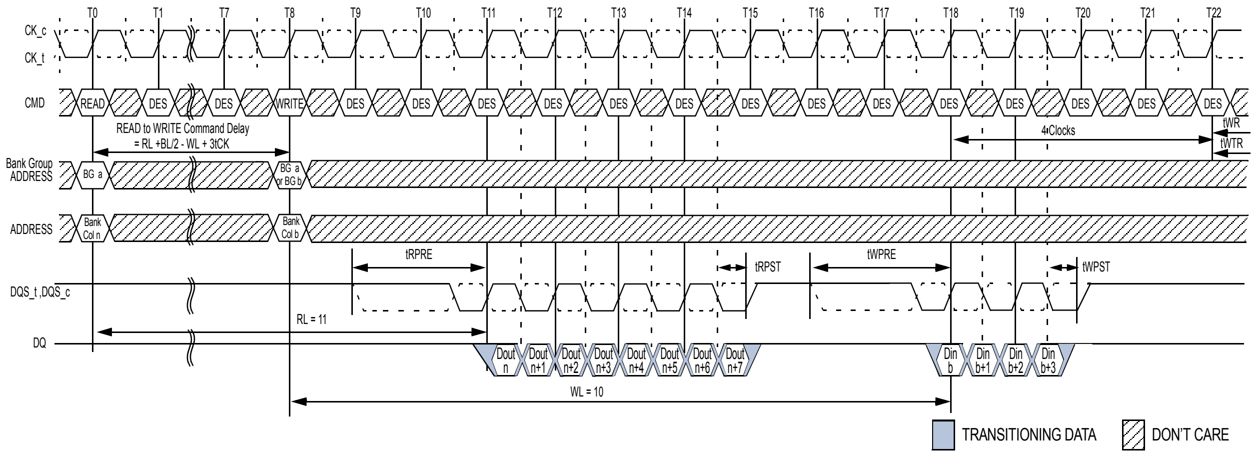
NOTE :
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 89. READ (BC4) to WRITE (BL8) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE :
1. BL = 8, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T8.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 90. READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE :
1. BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T8.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

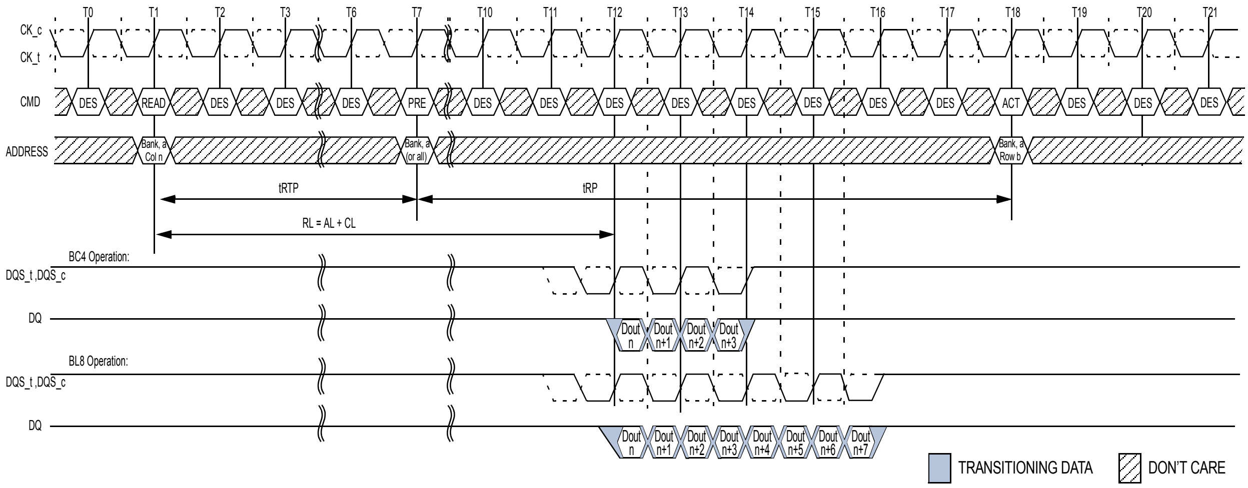
Figure 91. READ (BL8) to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group

2.24.3 Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to AL + tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by tRTP.min, A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

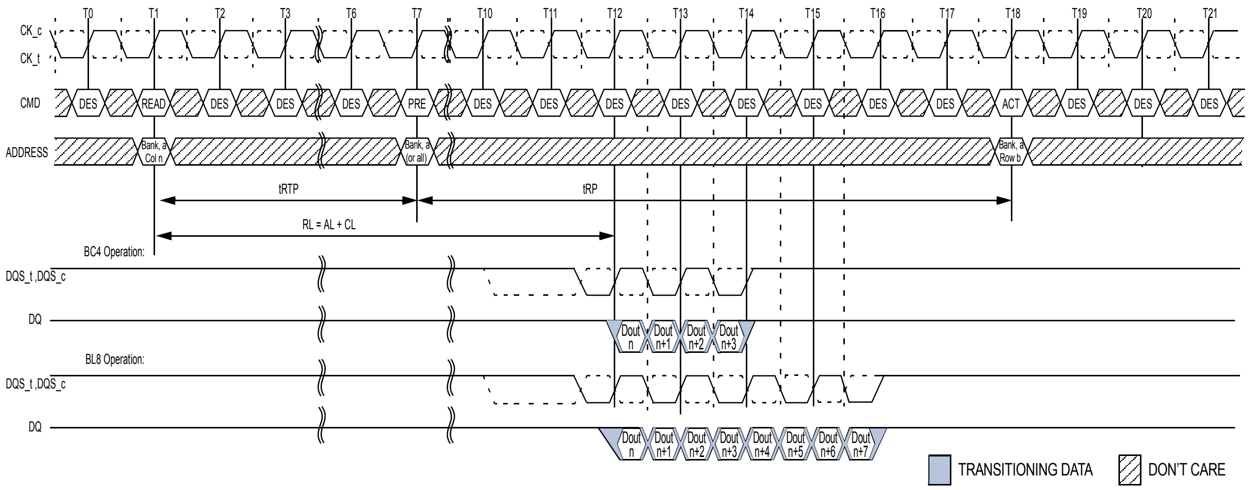
1. The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are show in Figure 92 to Figure 94.



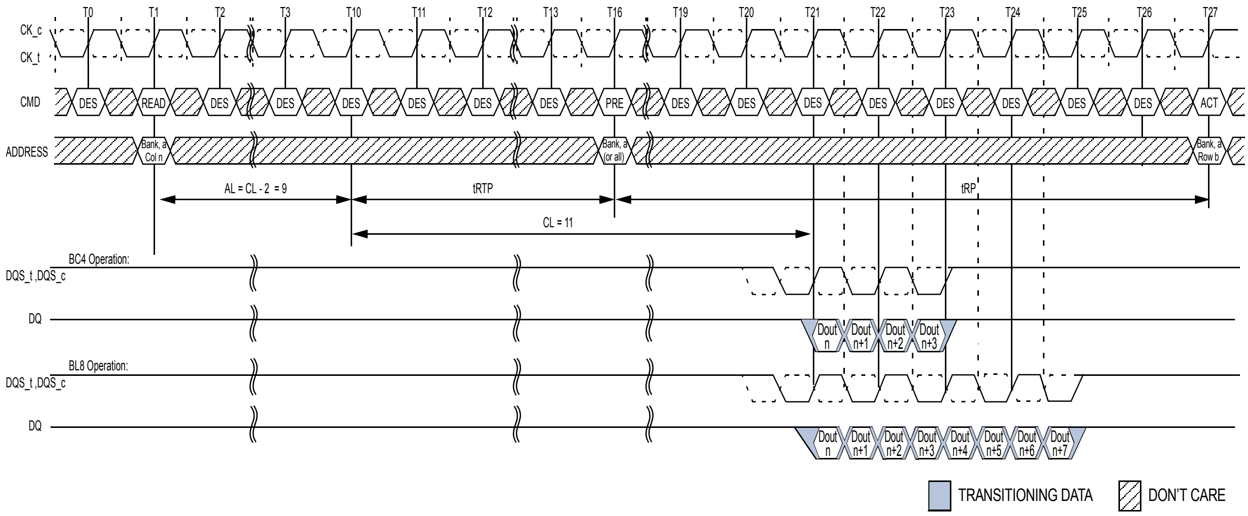
NOTE :
1. BL = 8, RL = 11(CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 92. READ to PRECHARGE with 1tCK Preamble



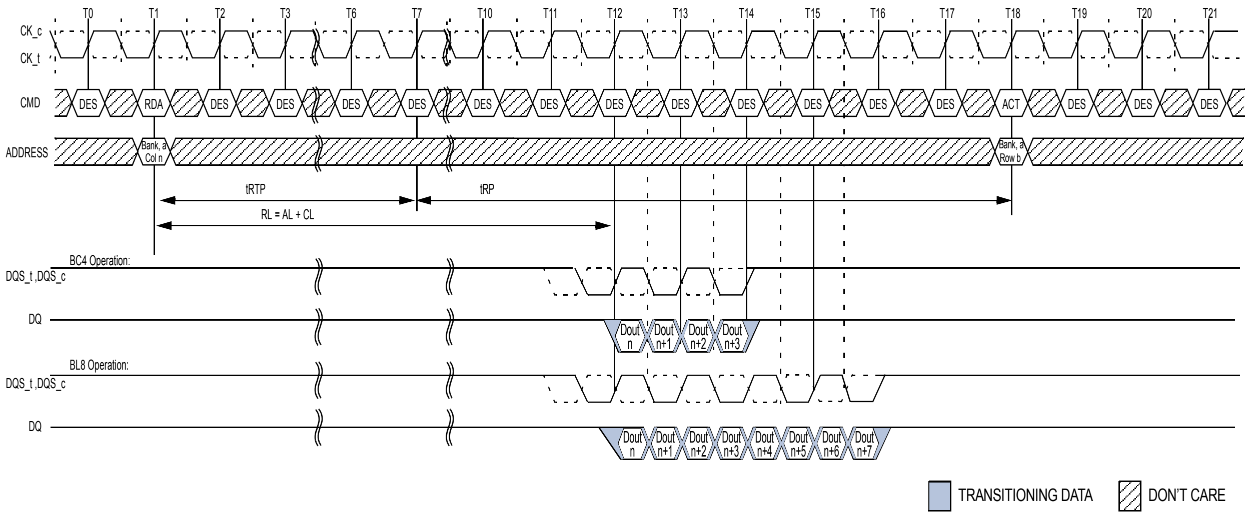
NOTE :
1. BL = 8, RL = 11(CL = 11 , AL = 0), Preamble = 2tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 93. READ to PRECHARGE with 2tCK Preamble



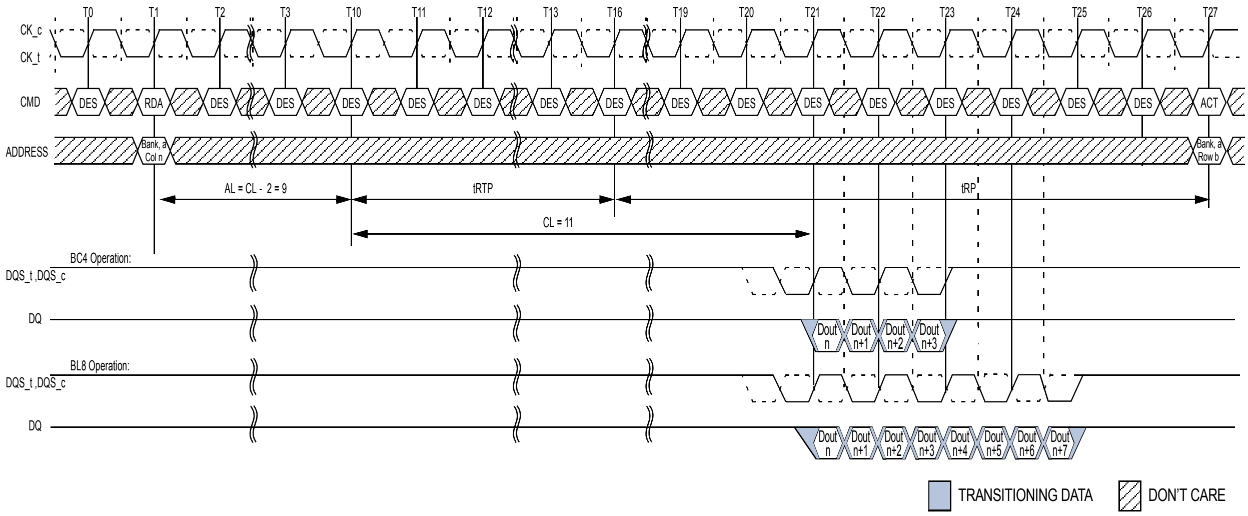
NOTE :
1. BL = 8, RL = 20 (CL = 11 , AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T16) and that tRC. MIN is satisfied at the next Active command time(T27).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 94. READ to PRECHARGE with Additive Latency and 1tCK Preamble



NOTE :
1. BL = 8, RL = 11 (CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[A11:9 = 001]
5. The example assumes tRC. MIN is satisfied at the next Active command time(T18).
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

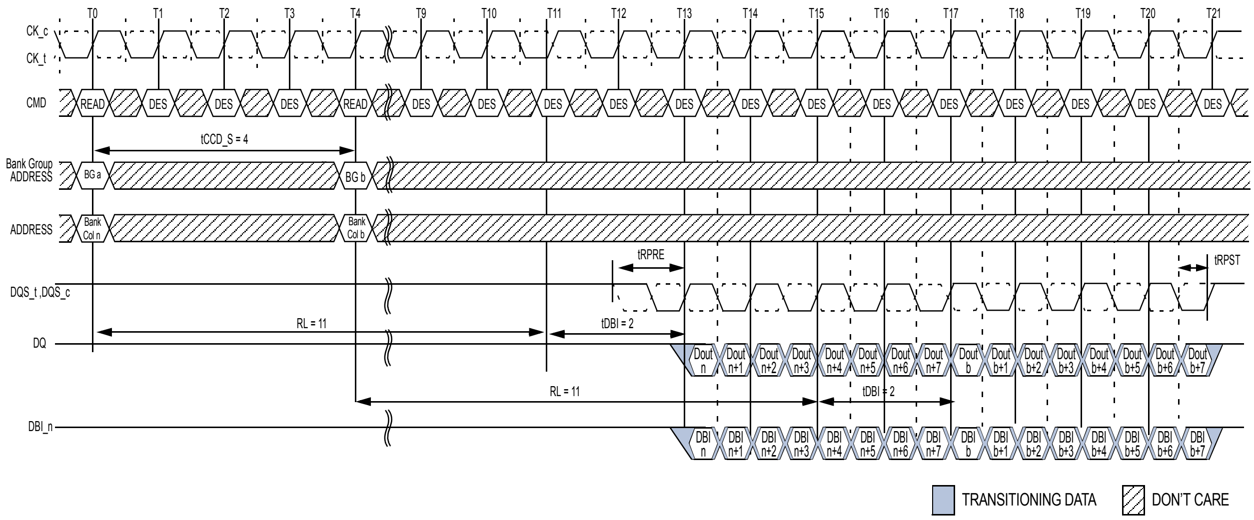
Figure 95. READ with Auto Precharge and 1tCK Preamble



NOTE :
1. BL = 8, RL = 20 (CL = 11 , AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[A11:9 = 001]
5. The example assumes tRC. MIN is satisfied at the next Active command time(T27).
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 96. READ with Auto Precharge, Additive Latency and 1tCK Preamble

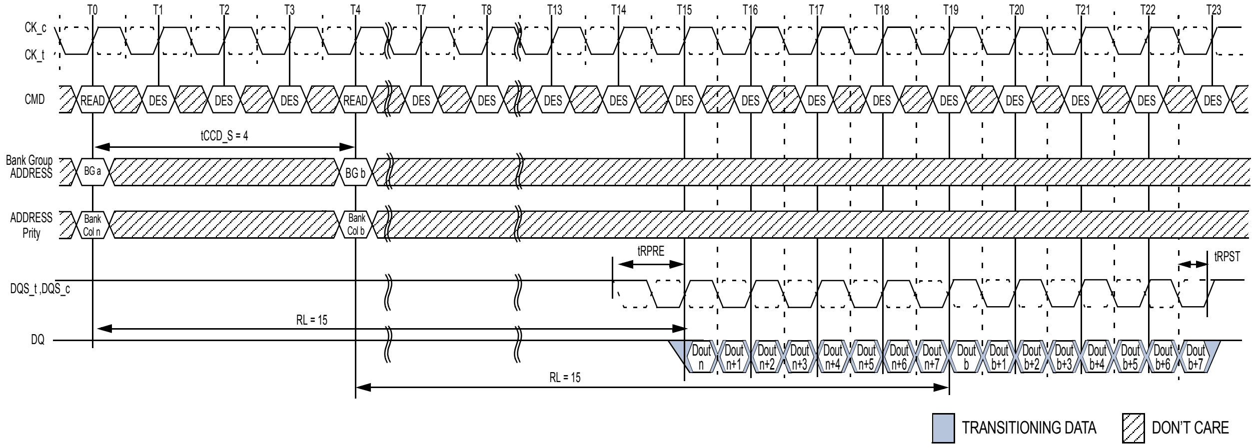
2.24.4 Burst Read Operation with Read DBI (Data Bus Inversion)



NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tDBI = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustrat:ion; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 00] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Enable.

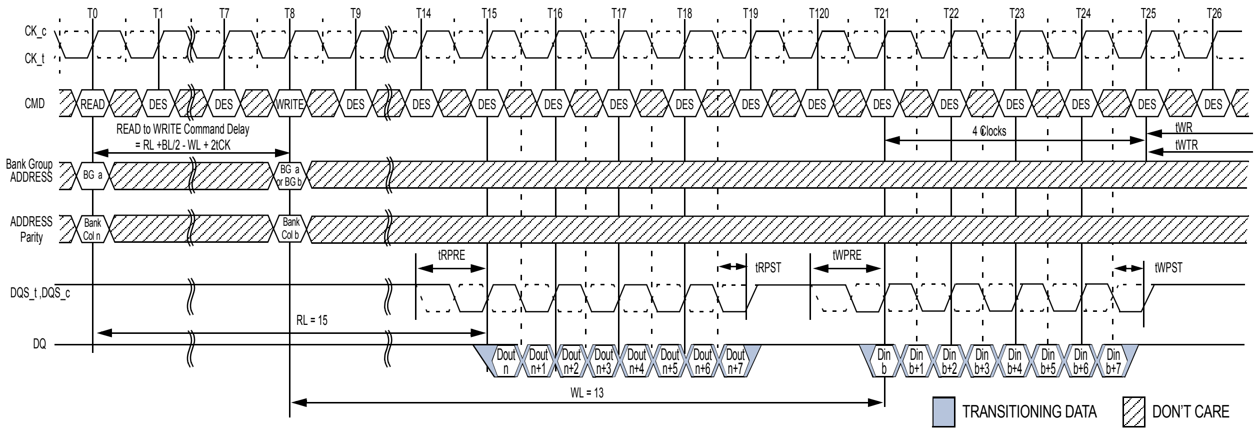
Figure 97. Consecutive READ (BL8) with 1tCK Preamble and DBI in Different Bank Group

2.24.5 Burst Read Operation with Command/Address Parity



NOTE :
1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.
5. CA Parity =Enable, CS to CA Latency = Disable, Read DBI = Disable.

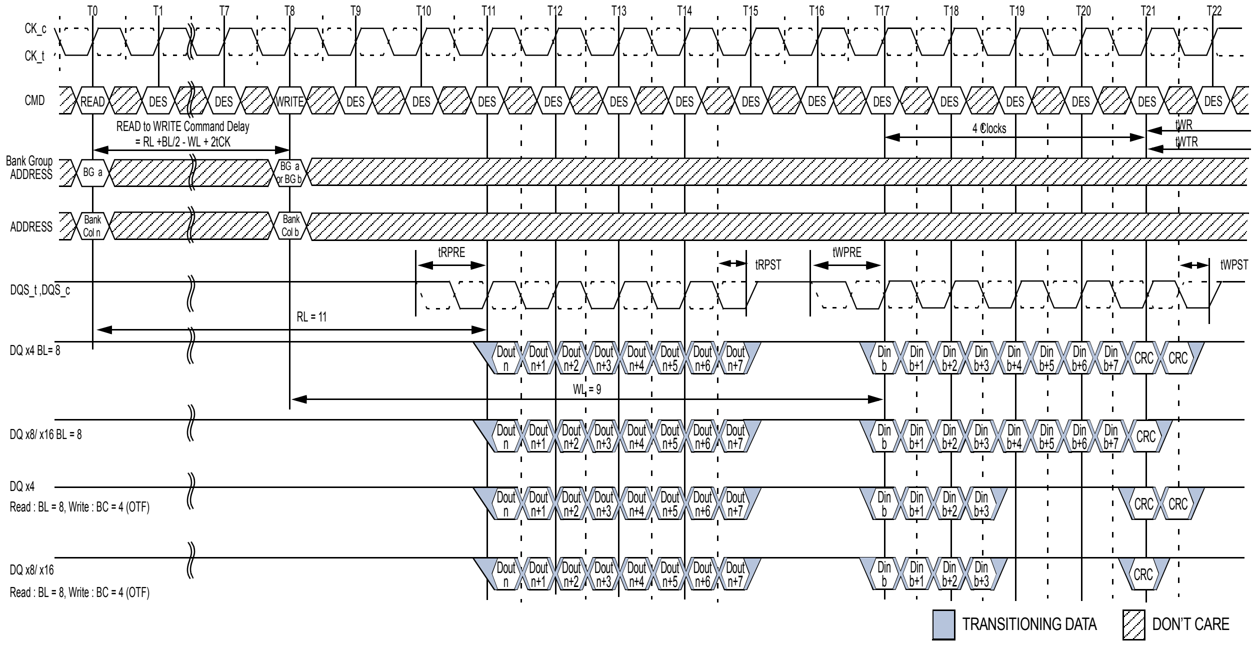
Figure 98. Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE :
1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Read Preamble = 1tCK, CWL=9, AL=0, PL=4, (WL=CL+AL+PL=13), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.
5. CA Parity = Enable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

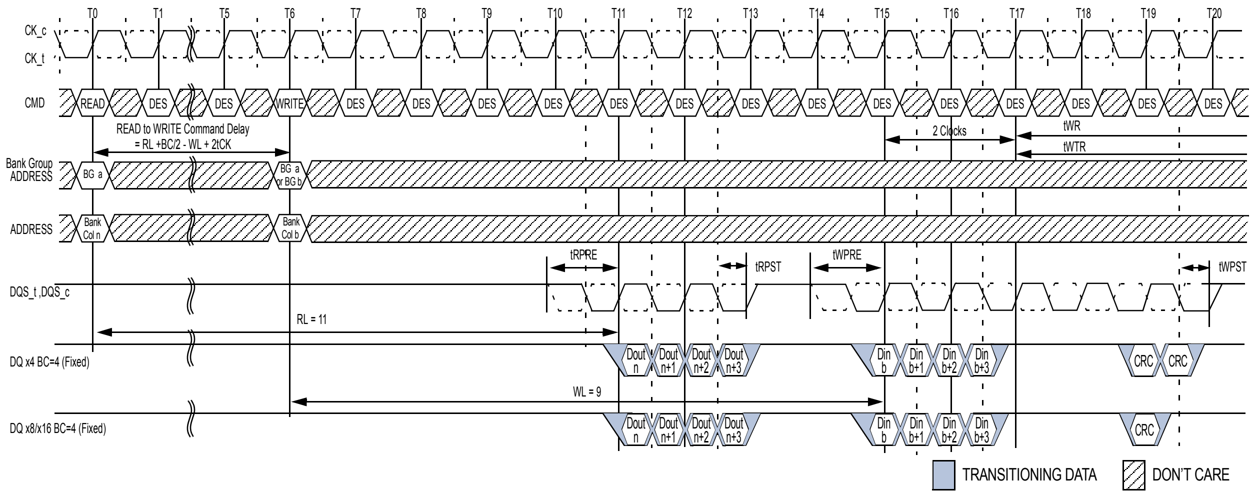
Figure 99. READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA parity in Same or Different Bank Group

2.24.6 Read to Write with Write CRC



NOTE :
1. BL = 8 (or BC = 4 : OTF for Write), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n . DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.
5. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during Write command at T8.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

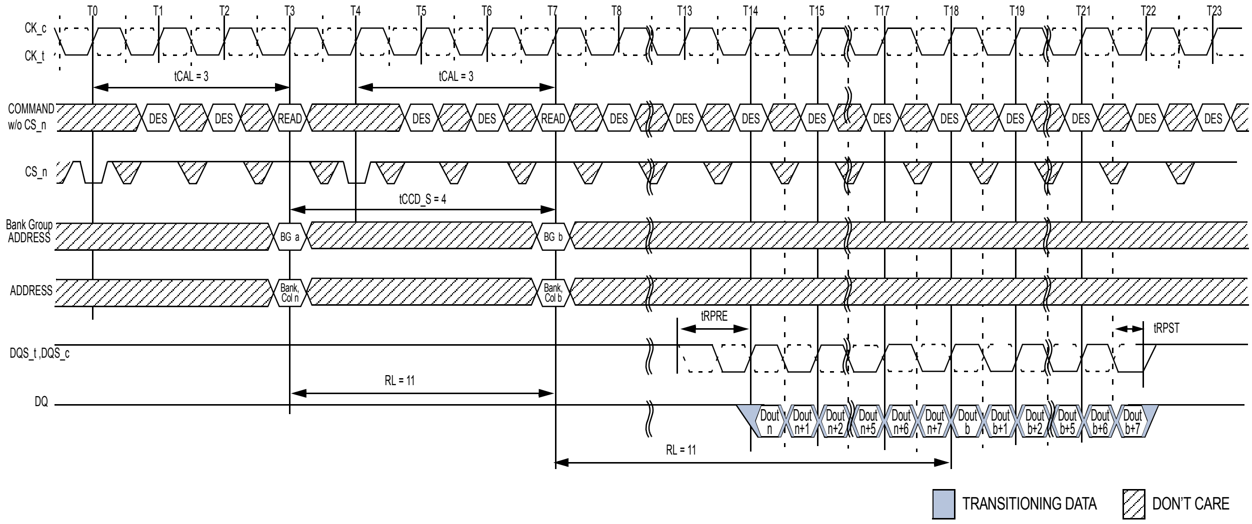
Figure 100. READ (BL8) to WRITE (BL8 or BC4:OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE :
1. BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n . DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

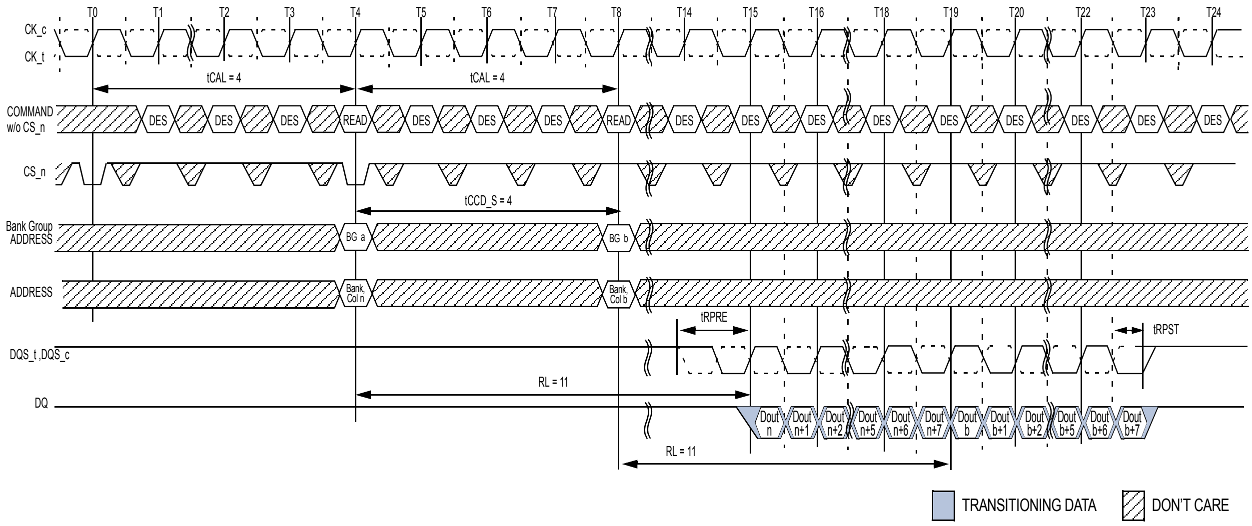
Figure 101. READ (BC4:Fixed) to WRITE (BC4:Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group

2.24.7 Read to Read with CS to CA Latency



NOTE :
1. BL = 8 ,AL = 0, CL = 11, CAL = 3, Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T3 and T7.
5. CA Parity = Disable, CS to CA Latency = Enable, Read DBI = Disable.
6. Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/ address bus as when CAL is disabled.

Figure 102. Consecutive READ (BL8) with CAL(3) and 1tCK Preamble in Different Bank Group



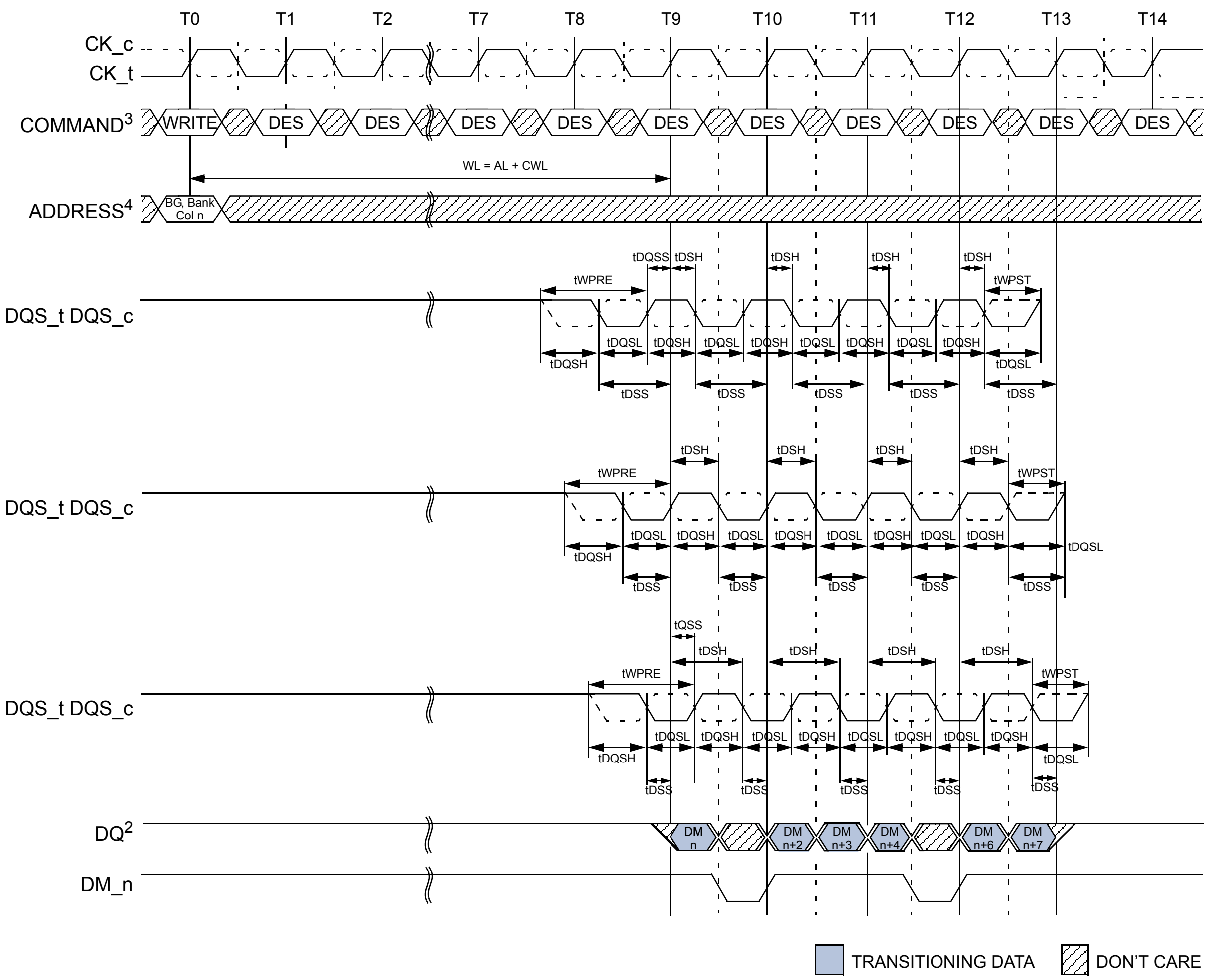
NOTE :
1. BL = 8 ,AL = 0, CL = 11, CAL = 4, Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4 and T8.
5. CA Parity = Disable, CS to CA Latency = Enable, Read DBI = Disable.
6. Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/ address bus as when CAL is disabled.

Figure 103. Consecutive READ (BL8) with CAL(4) and 1tCK Preamble in Different Bank Group

2.25 Write Operation

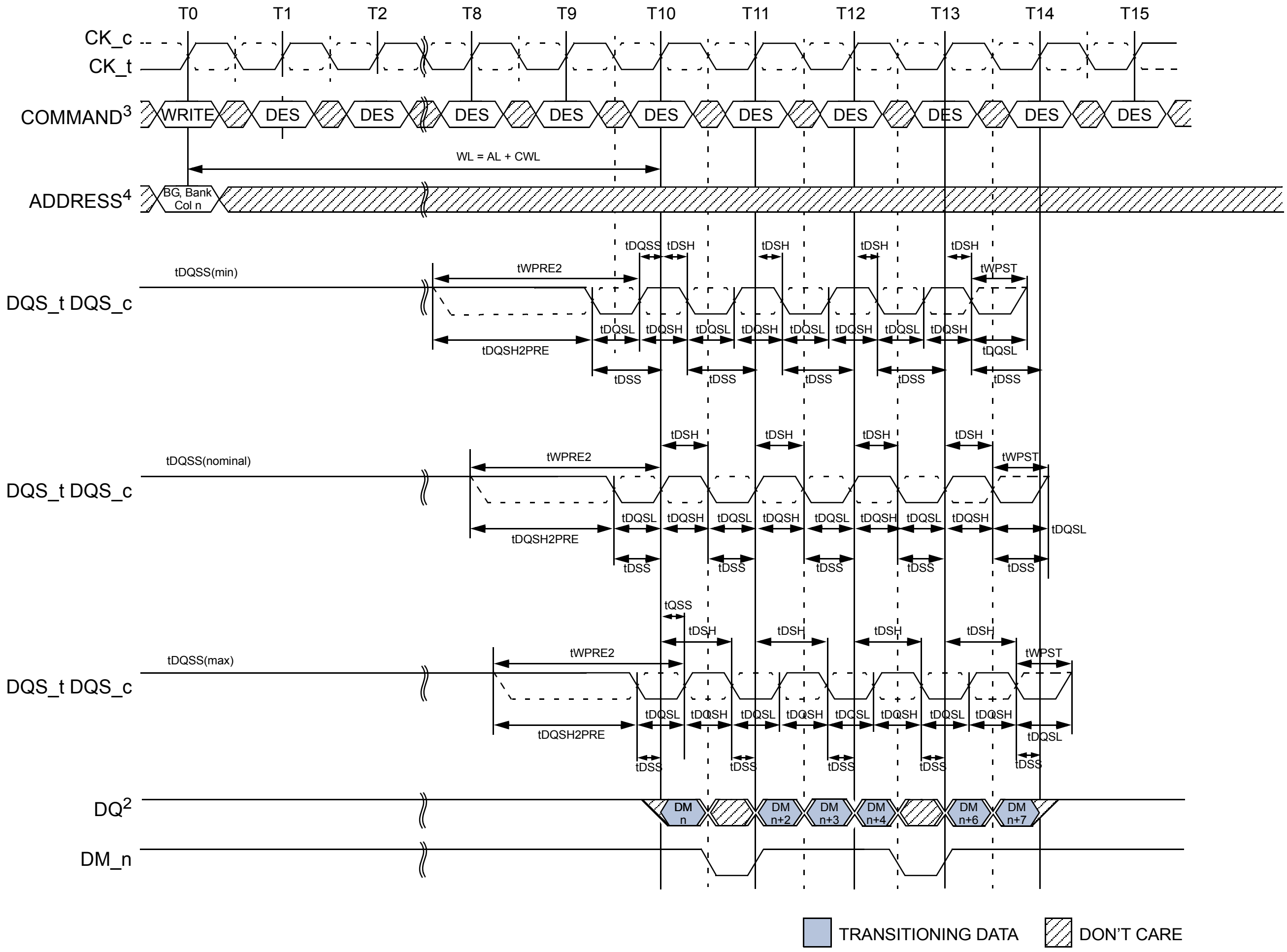
2.25.1 Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that "belong" to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).



NOTE 1. BL8, WL=9 (AL=0, CWL=9)
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration : other commands may be valid at these times.
4. BL8 stting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12=1 during WRITE command at T0.
5. tDQSS must be met at each rising clock edge.

Figure 104. Write Timing Definition and Parameters with 1tCK Preamble



NOTE 1. BL8, WL=9 (AL=0, CWL=9)
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration : other commands may be valid at these times.
4. BL8 stting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12=1 during WRITE command at T0.
5. tDQSS must be met at each rising clock edge.

Figure 105. Write Timing Definition and Parameters with 2tCK Preamble

2.25.2 Write Data Mask

One write data mask (DM_n) pin for each 8 data bits (DQ) will be supported on DDR4 SDRAMs, consistent with the implementation on DDR3 SDRAMs. It has identical timings on write operations as the data bits as shown in ure AA and BB, and though used in a unidirectional manner, is internally loaded identically to data bits to ensure matched system timing. DM_n is not used during read cycles for any bit organizations including x4, x8, and x16, however, DM_n of x8 bit organization can be used as TDQS_t during write cycles if enabled by the MR1[A11] setting and x8 /x16 organization as DBI_n during write cycles if enabled by the MR5[A11] setting. See "TDQS_t, TDQS_c" on page TBD for more details on TDQS vs. DM_n operations and DBI_n on page TBD for more detail on DBI_n vs. DM_n operations.

2.25.3 tWPRE Calculation

The method for calculating differential pulse widths for tWPRE is shown in Figure 106.

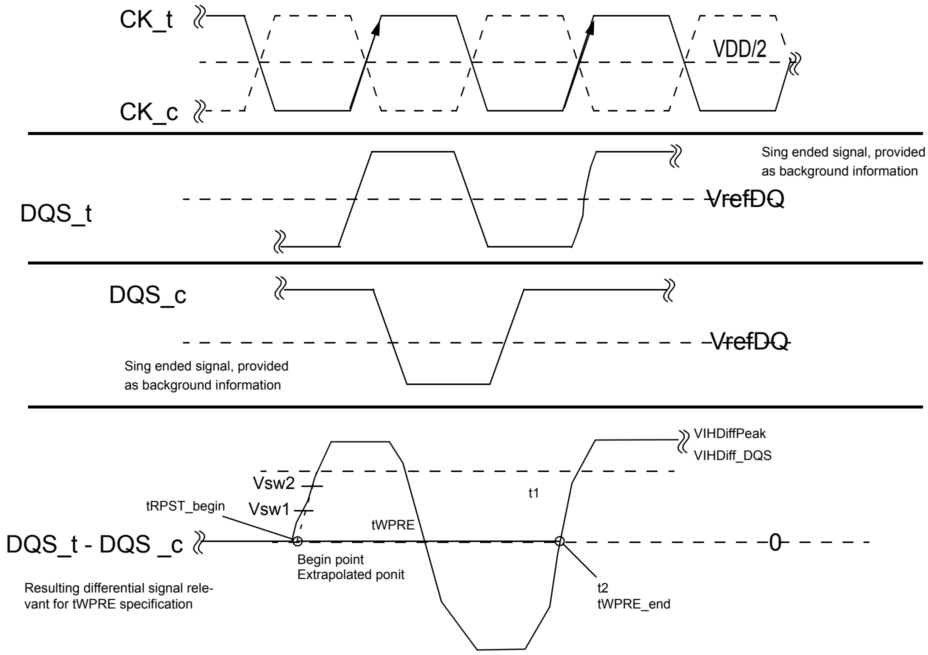


Figure 106. Method for calculating tWPRE transitions and endpoints

[Table 58] Reference Voltage for tWPRE Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQS_t, DQS_c differential WRITE Preamble	tWPRE	VIHDiff_DQS x 0.1	VIHDiff_DQS x 0.9	

The method for calculating differential pulse widths for tWPRE2 is same as tWPRE.

2.25.4 tWPST Calculation

The method for calculating differential pulse widths for tWPST is shown inFigure 107.

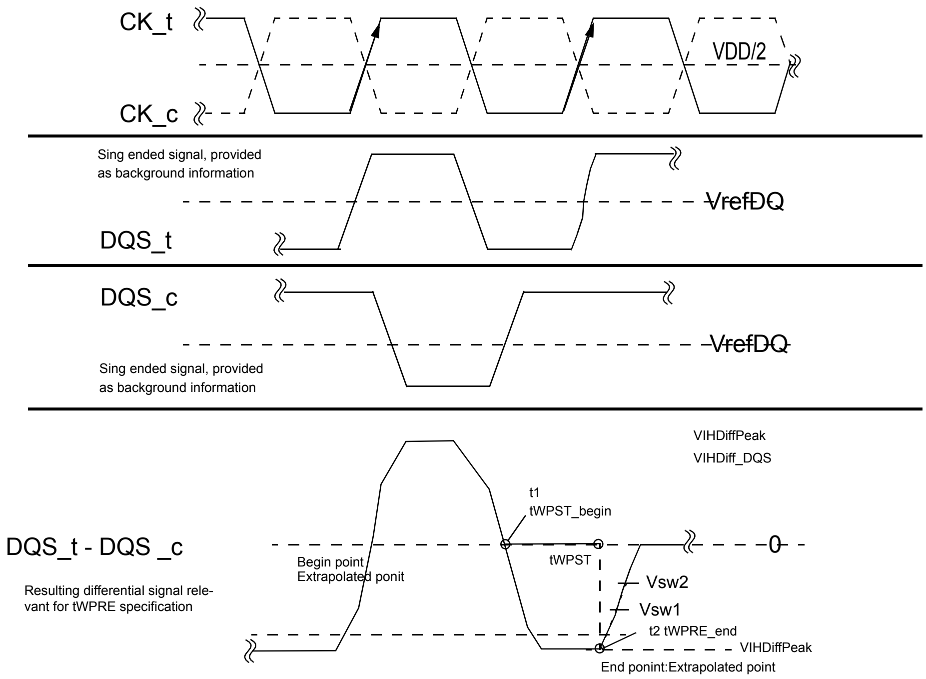


Figure 107. Method for calculating tWPST transitions and endpoints

[Table 59] Reference Voltage for tWPST Timing Measurements

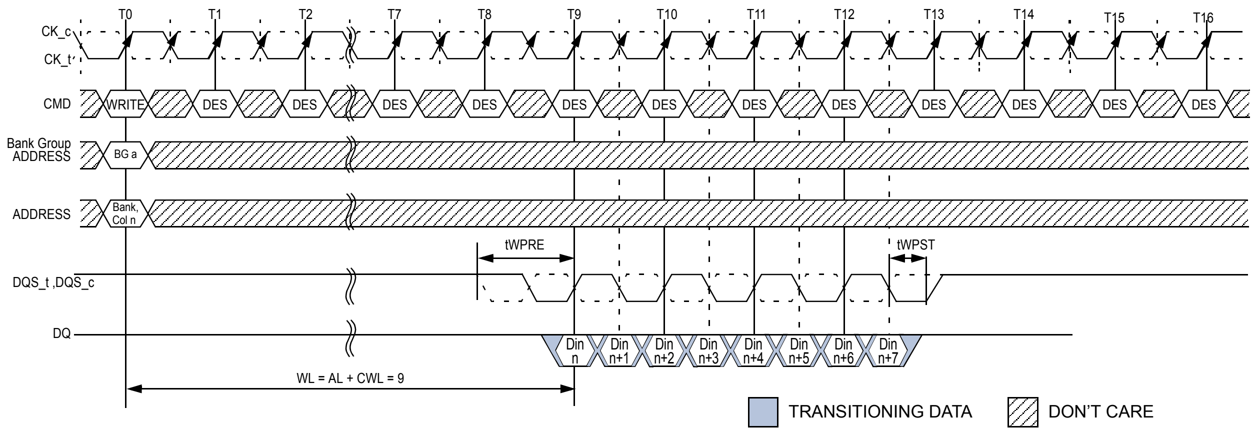
Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQS_t, DQS_c differential WRITE Postamble	tWPST	VILDiff_DQS x 0.9	VILDiff_DQS x 0.1	

[Table 60] Timing Parameters by Speed Grade

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c differential WRITE Preamble (1tCK Preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)	
DQS_t, DQS_c differential WRITE Preamble (2tCK Preamble)	tWPRE2	-	-	-	-	-	-	-	-	tCK(avg)	
DQS_t, DQS_c differential WRITE Postamble	tWPST	TBD	-	TBD	-	TBD	-	TBD	-	tCK(avg)	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
DQS_t, DQS_c differential input high pulse width at 2tCK Preamble	tDQSH2PRE	-	-	-	-	-	-	-	-	tCK(avg)	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1tCK Preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK(avg)	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK(avg)	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK(avg)	

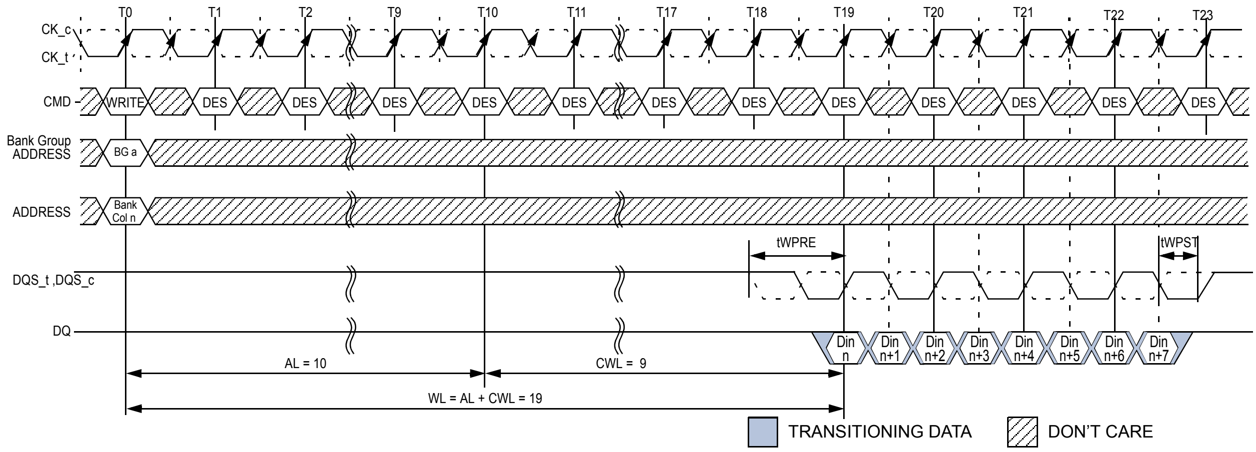
2.25.5 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.



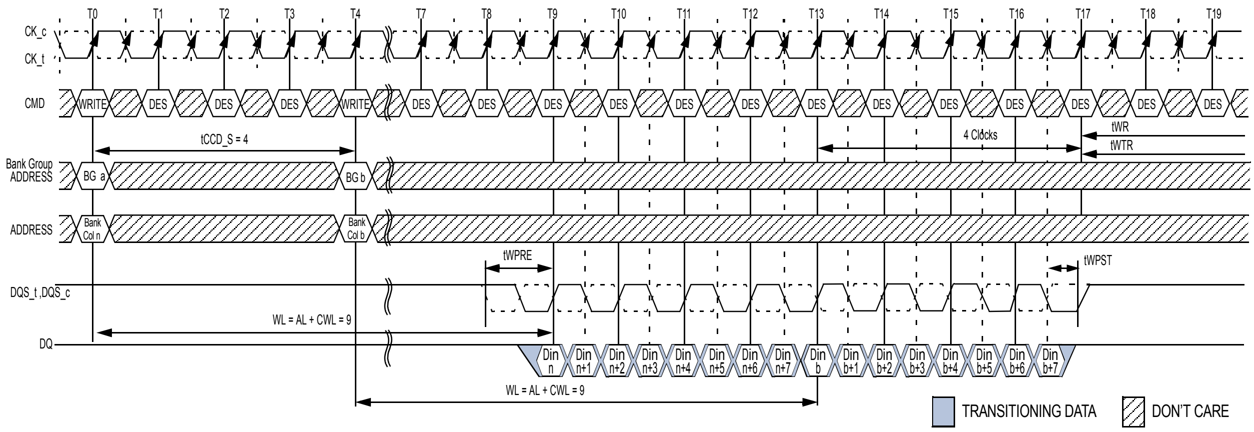
NOTE :
1. BL = 8 ,WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

Figure 108. WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)



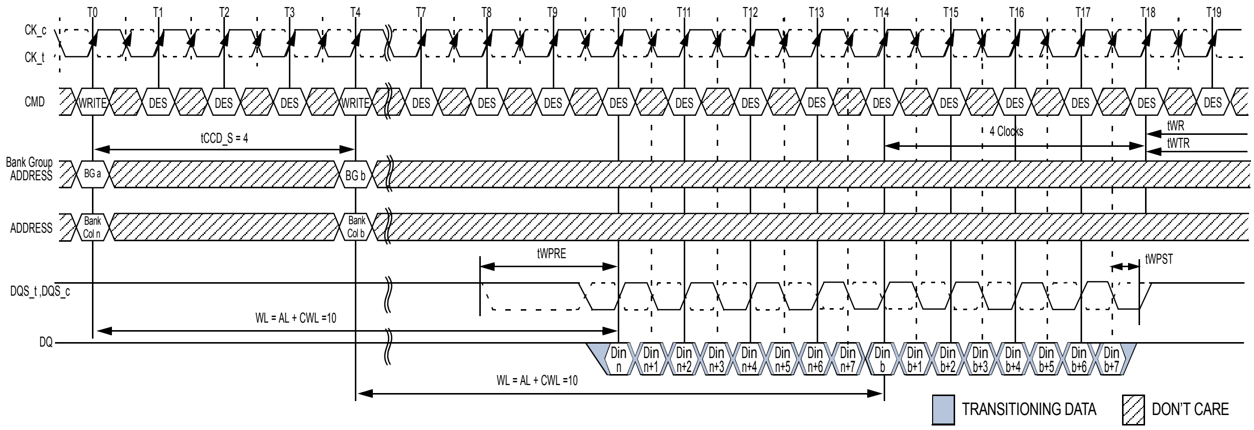
NOTE :
1. BL = 8 ,WL = 19, AL = 10 (CL-1), CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

Figure 109. WRITE Burst Operation WL = 19 (AL = 10, CWL = 9, BL8)



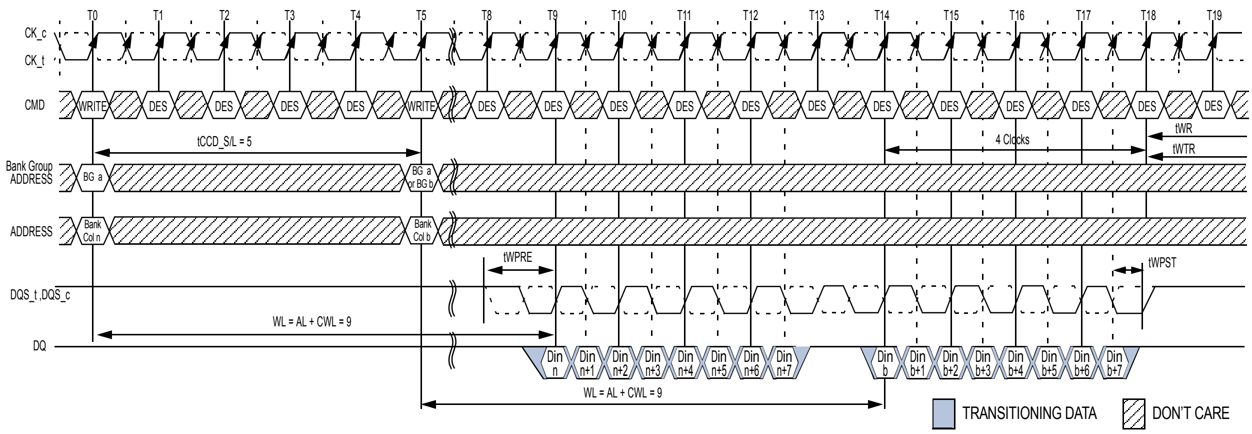
NOTE :
1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.
5. C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

Figure 110. Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group



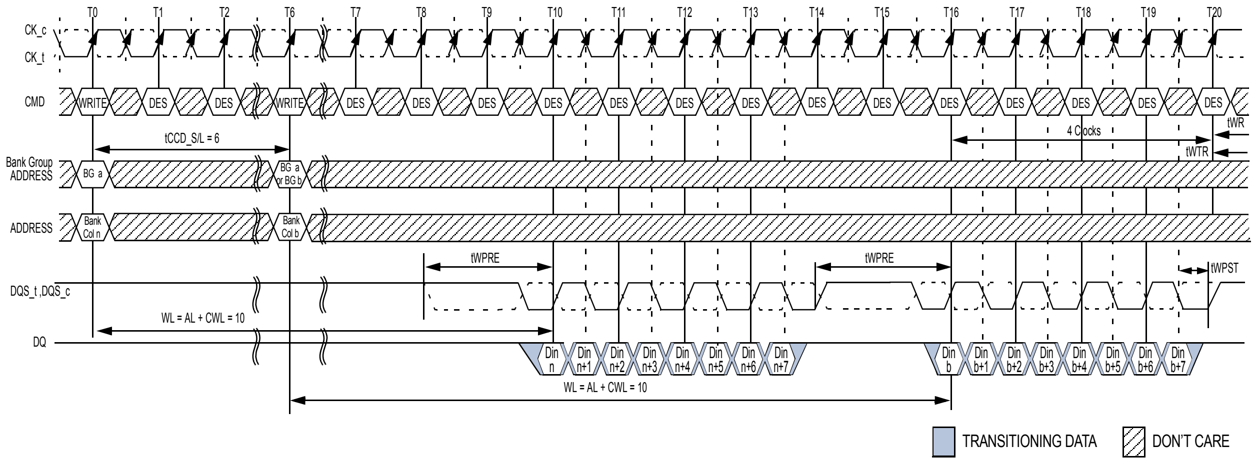
NOTE :
1. BL = 8 ,AL = 0, CWL = 9 + 1 = 10[7], Preamble = 2tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time(tWR) and write timing parameter(tWTR) are referenced from the first rising clock edge after the last write data shown at T18.
7. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

Figure 111. Consecutive WRITE (BL8) with 2tCK Preamble in Different Bank Group



NOTE:
1. BL = 8 ,AL = 0, CWL = 9 , Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T5.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

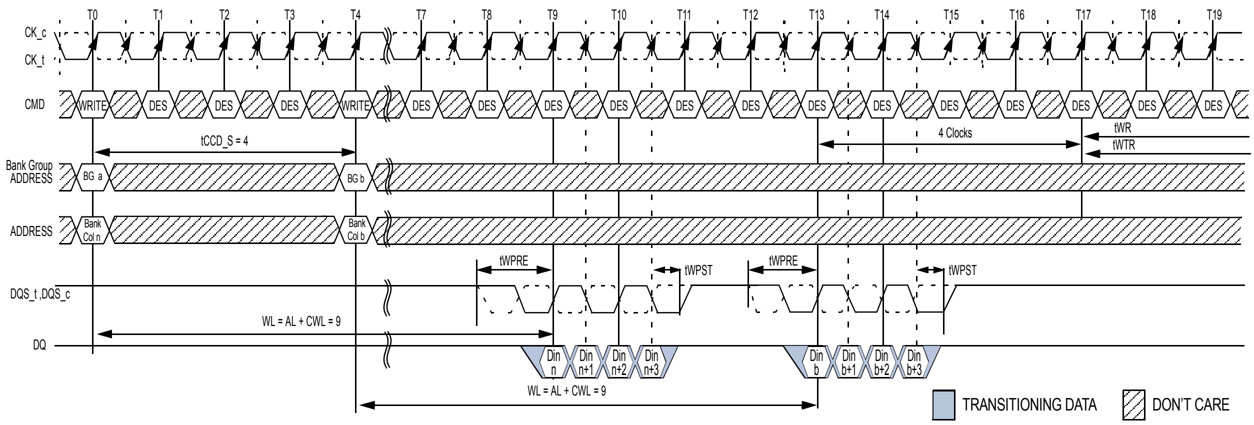
Figure 112. Nonconsecutive WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE:

1. BL = 8 ,AL = 0, CWL = 9 + 1 = 10[8] , Preamble = 2tCK, tCCD_S/L = 6
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. tCCD_S/L=5 isn't allowed in 2tCK preamble mode.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T20.
8. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

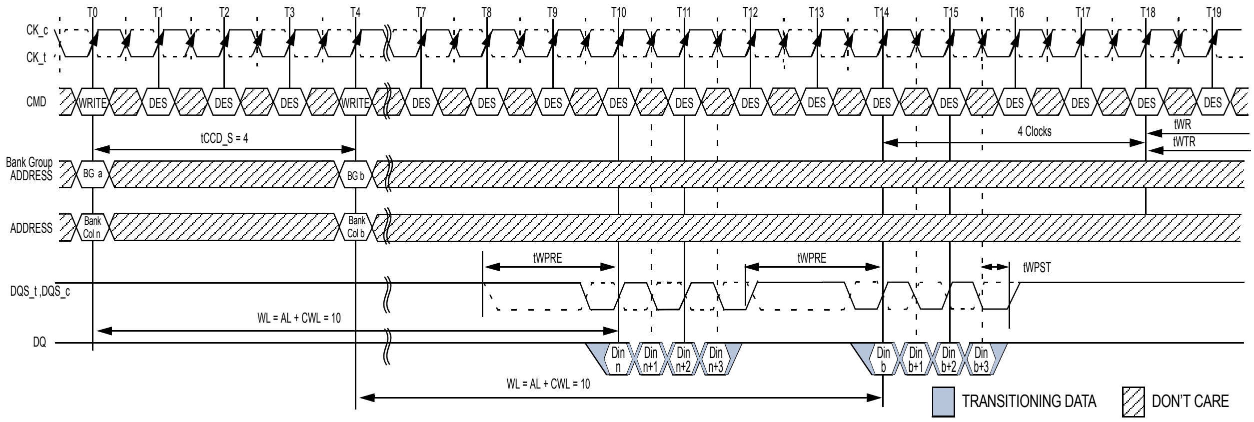
Figure 113. Nonconsecutive WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE:

1. BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

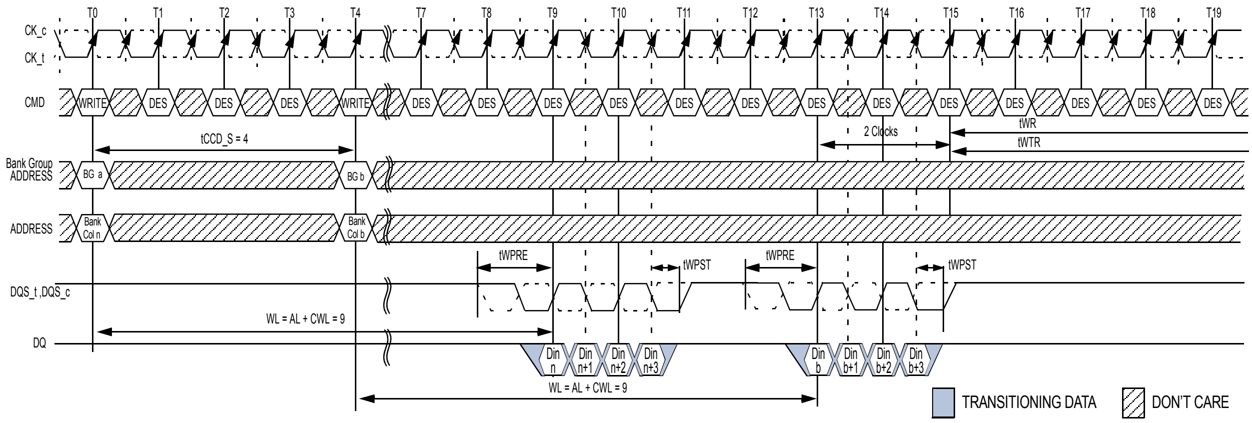
Figure 114. WRITE (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



NOTE:

1. BC = 4, AL = 0, CWL = 9 + 1 = 10[7] , Preamble = 2tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.
7. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

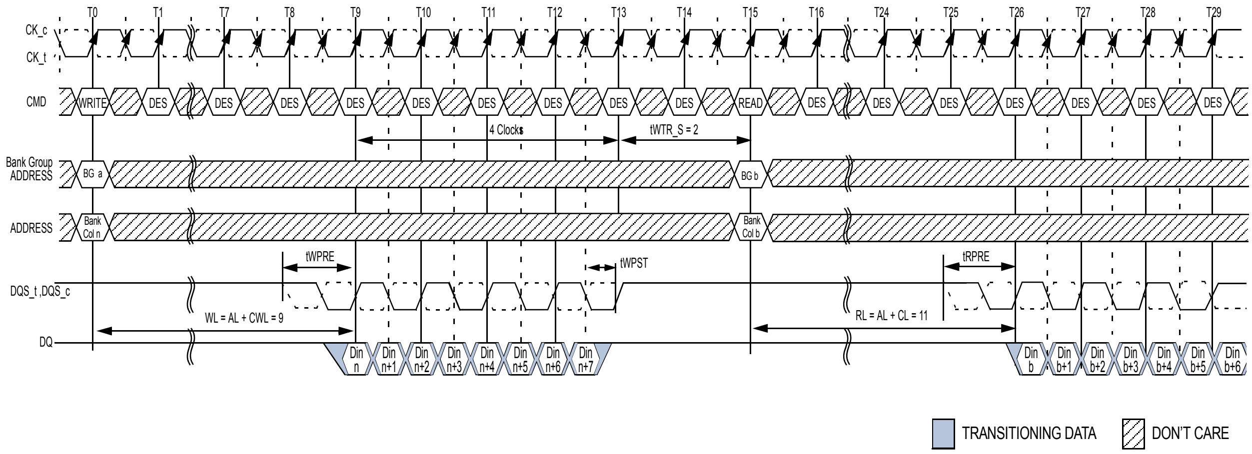
Figure 115. WRITE (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Different Bank Group



NOTE:

1. BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T15.

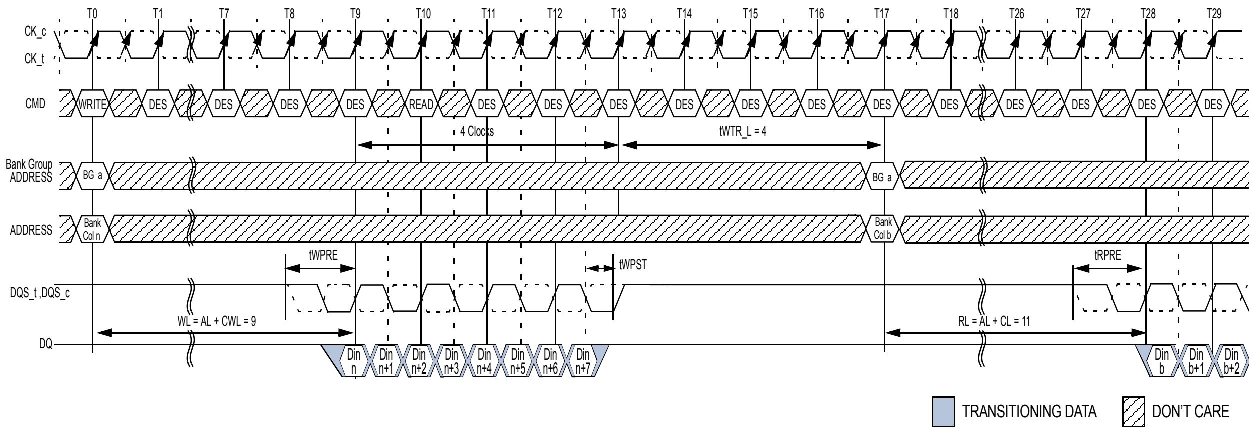
Figure 116. WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Different Bank Group



NOTE:

1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n(or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T15.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

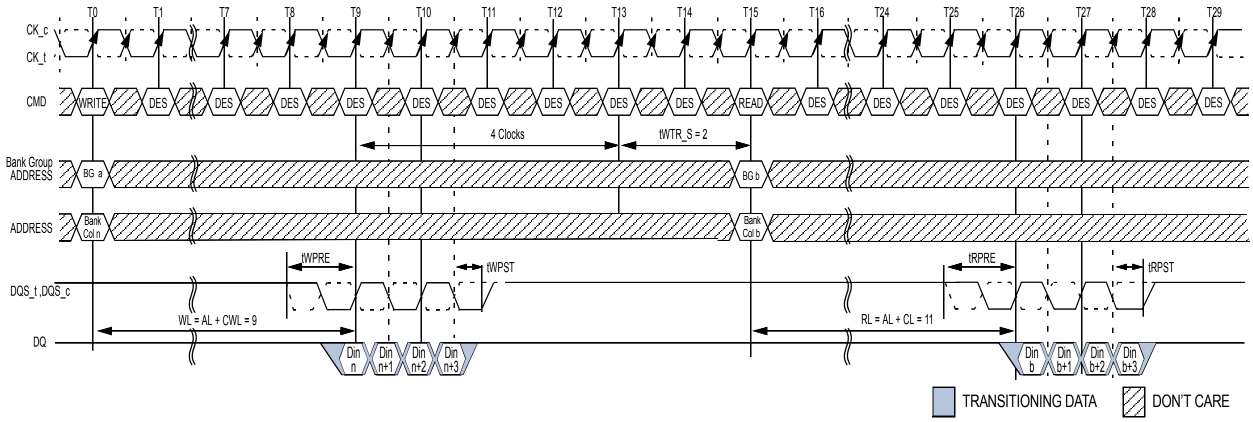
Figure 117. WRITE (BL8) to READ (BL8) with 1tCK Preamble in Different Bank Group



NOTE:

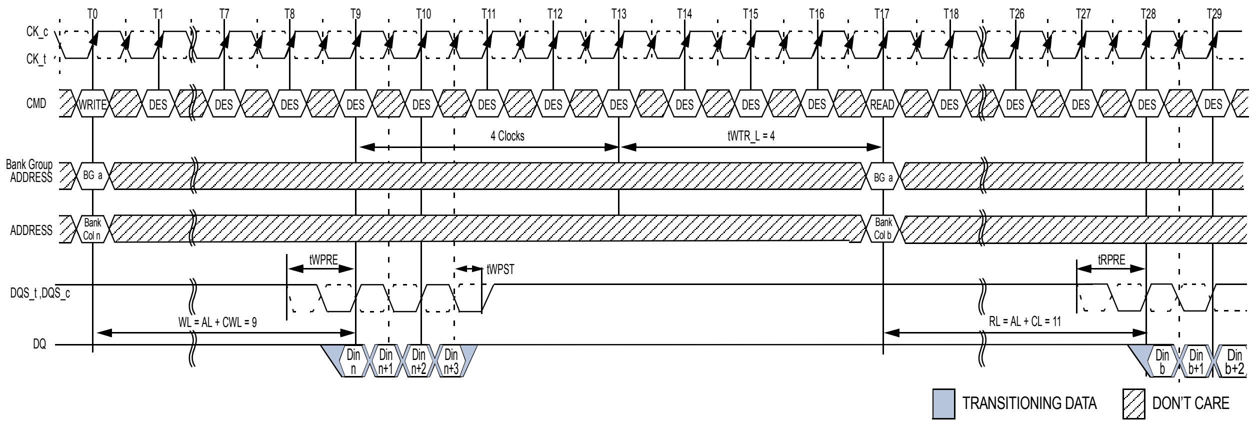
1. BL = 8, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T17.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 118. WRITE (BL8) to READ (BL8) with 1tCK Preamble in Same Bank Group



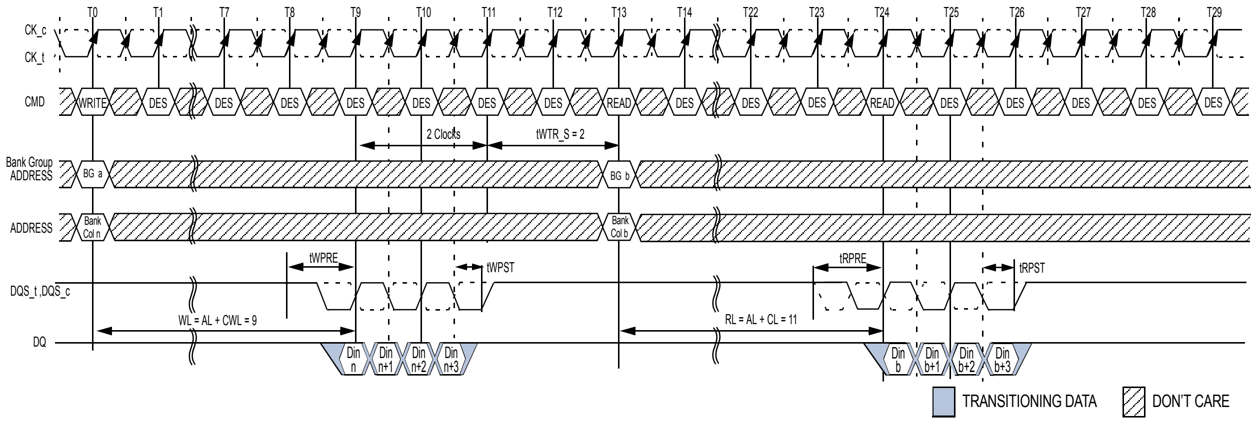
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T15.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 119. WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Different Bank Group



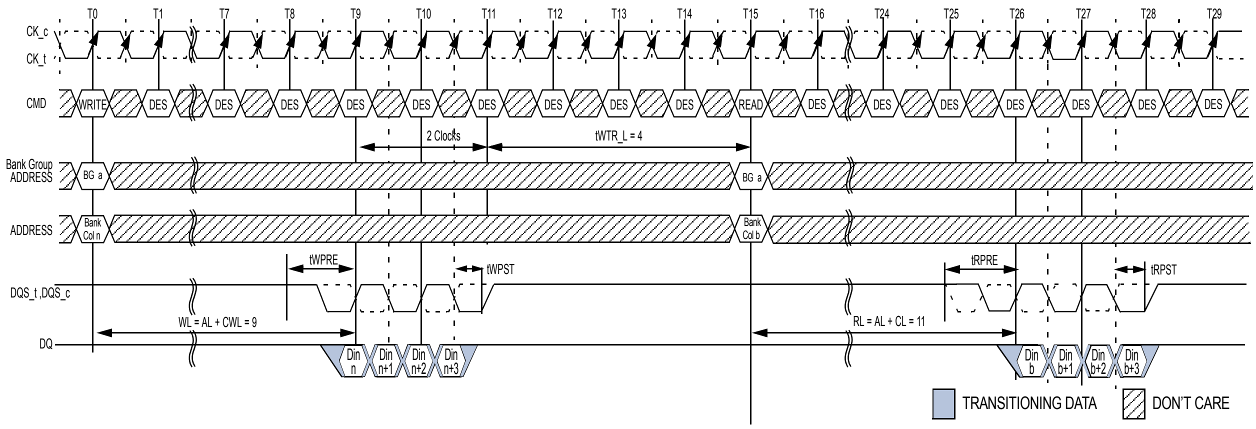
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T17.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 120. WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Same Bank Group



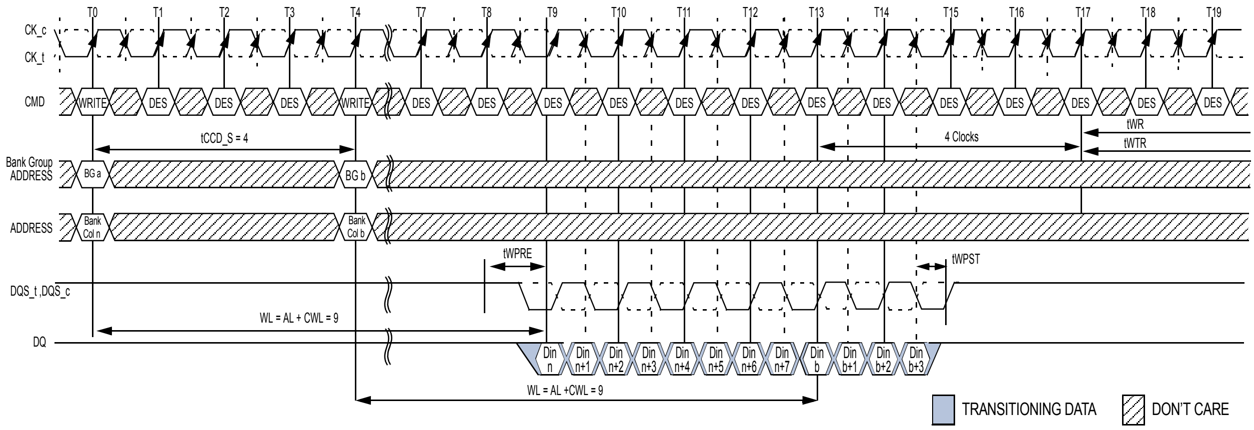
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T11.

Figure 121. WRITE (BC4)Fixed to READ (BC4)Fixed with 1tCK Preamble in Different Bank Group



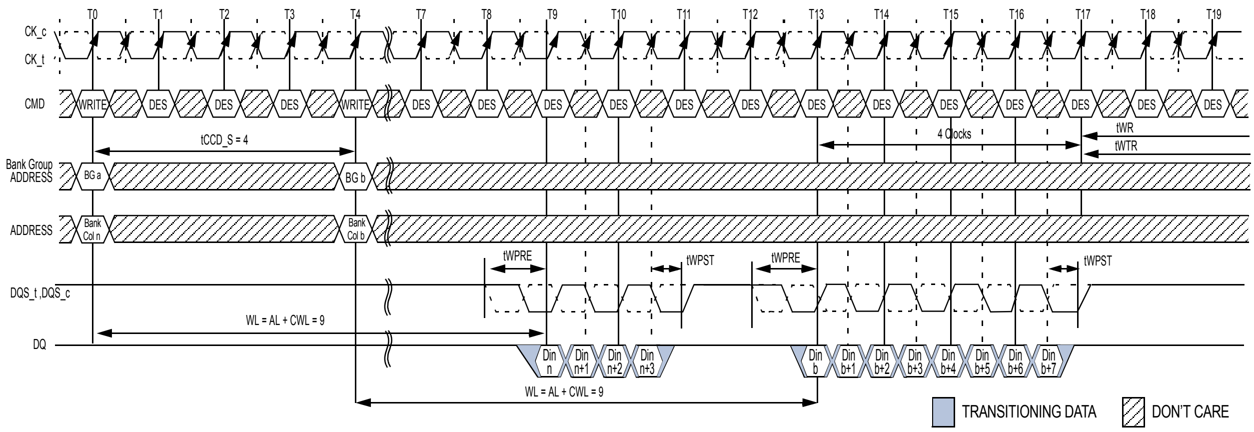
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T11.

Figure 122. WRITE (BC4)Fixed to READ (BC4)Fixed with 1tCK Preamble in Same Bank Group



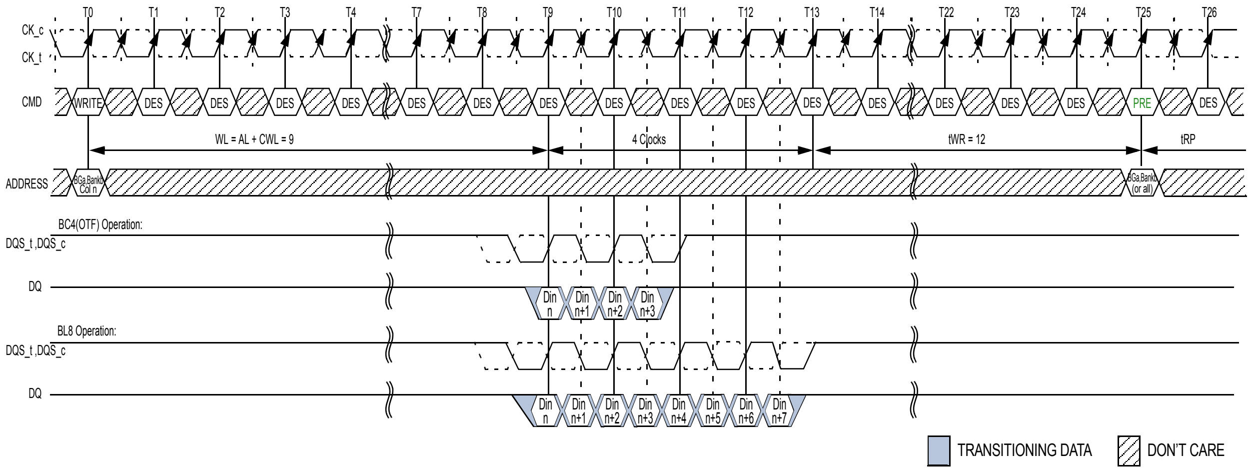
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

Figure 123. WRITE (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



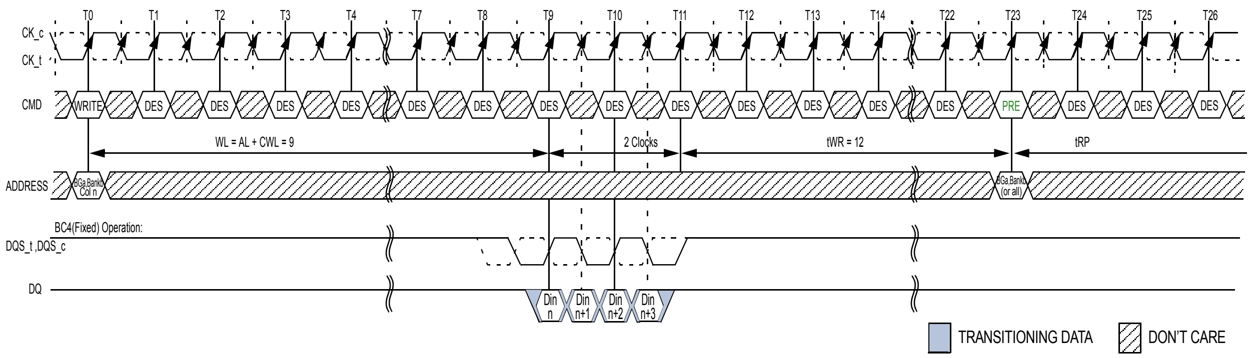
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

Figure 124. WRITE (BC4)OTF to WRITE (BL8) with 1tCK Preamble in Different Bank Group



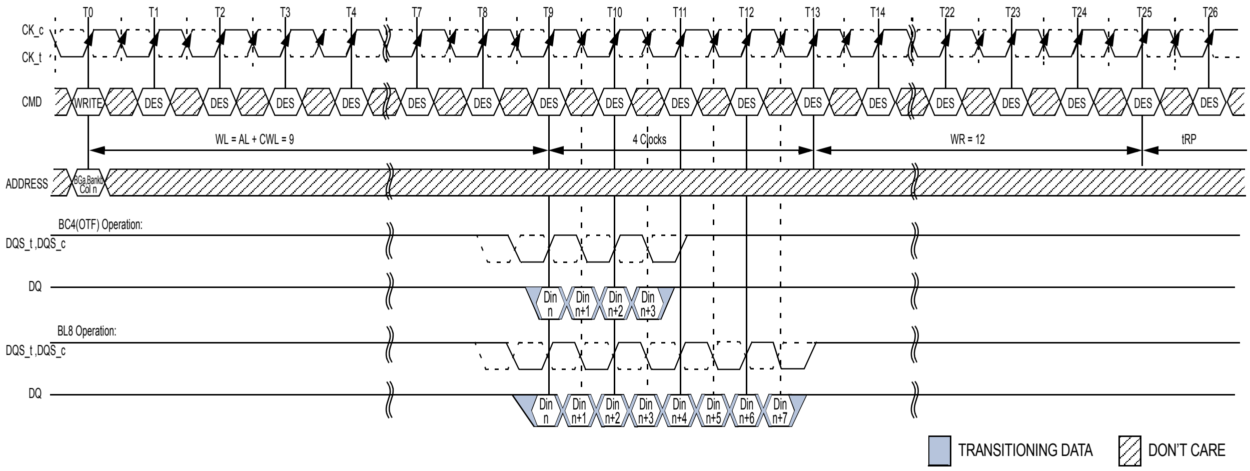
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:0] or MR0[A1:0 = 01] and A12 =1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13.
   tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 125. WRITE (BL8/BC4) OTF to PRECHARGE Operation with 1tCK Preamble



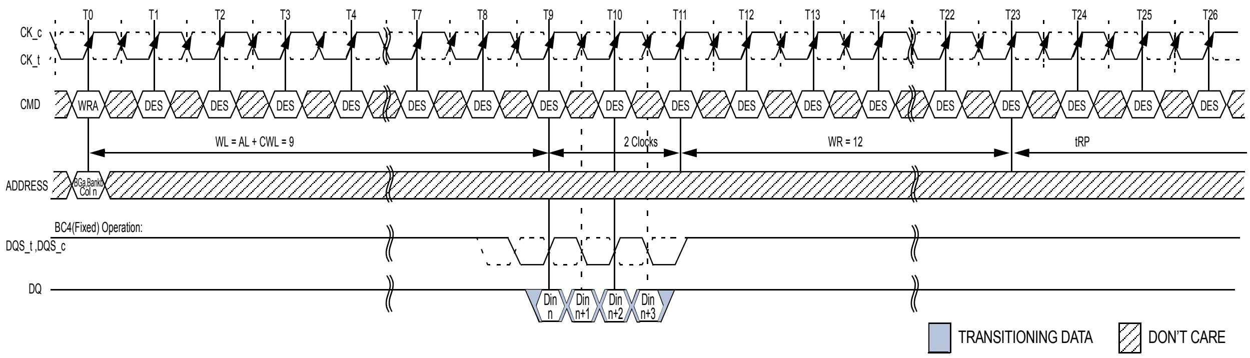
NOTE:
1. BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11.
   tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 126. WRITE (BC4) Fixed to PRECHARGE Operation with 1tCK Preamble



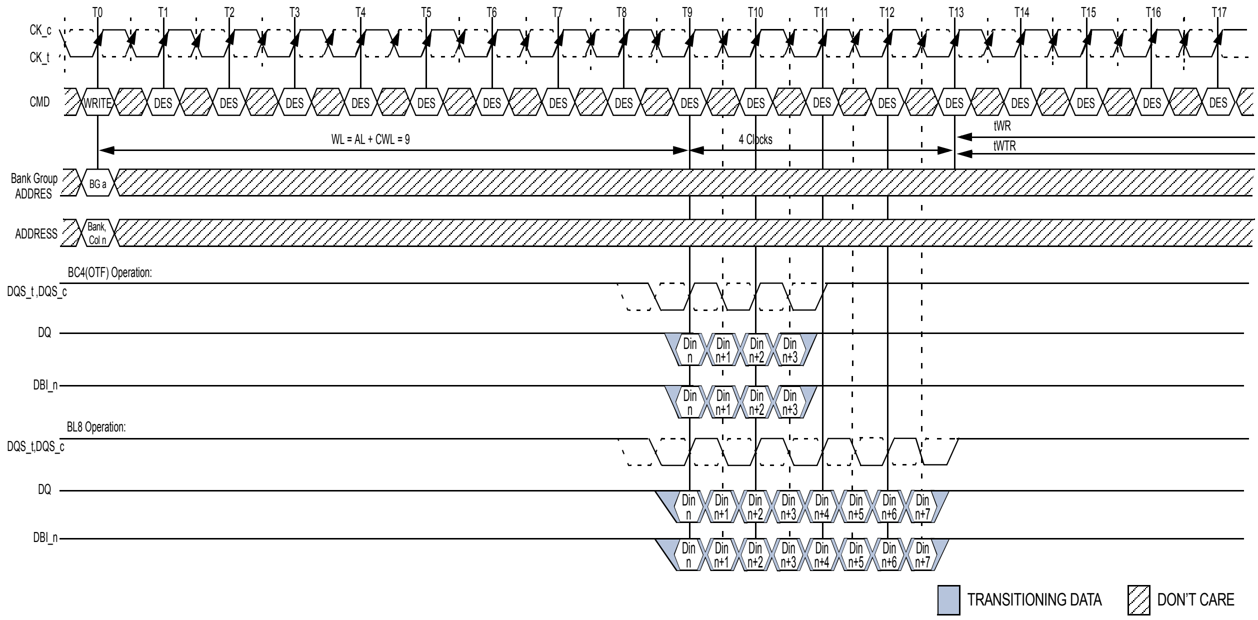
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 =1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (WR) is referenced from the first rising clock edge after the last write data shown at T13.
   WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 127. WRITE (BL8/BC4) OTF with Auto PRECHARGE Operation and 1tCK Preamble



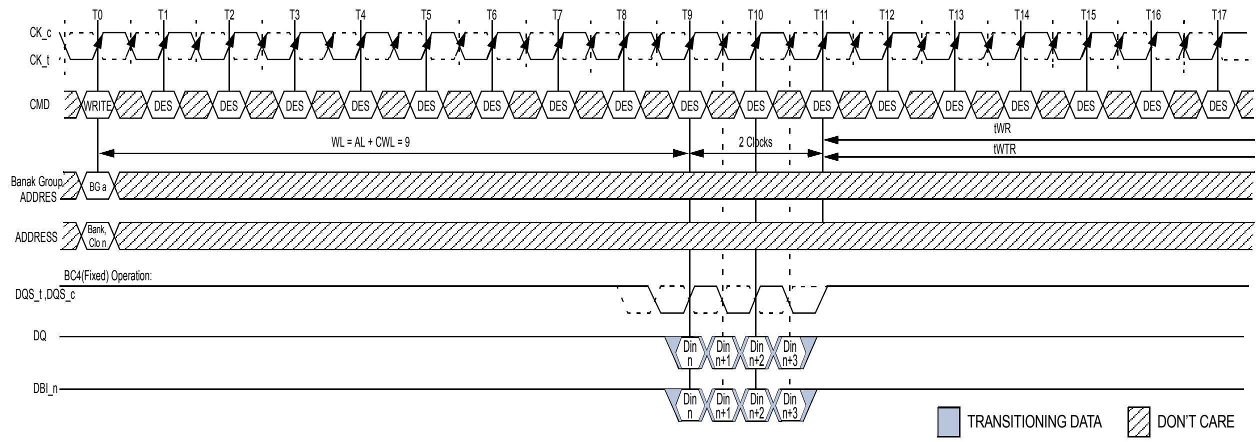
NOTE:
1. BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11.
   WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 128. WRITE (BC4) Fixed with Auto PRECHARGE Operation and 1tCK Preamble



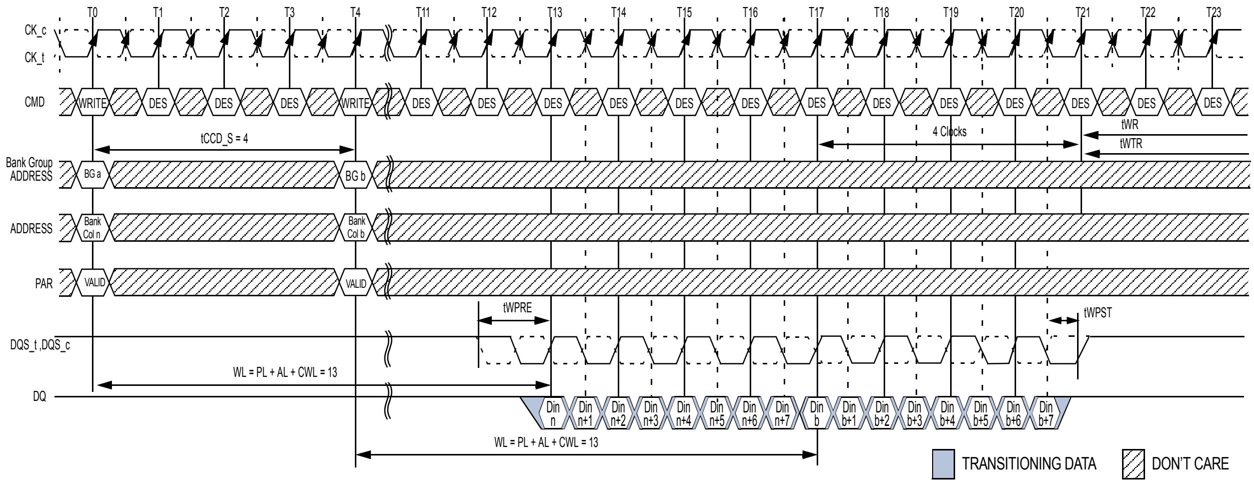
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.
6. The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 129. WRITE (BL8/BC4) OTF with 1tCK Preamble and DBI



NOTE:
1. BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.
6. The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T11.

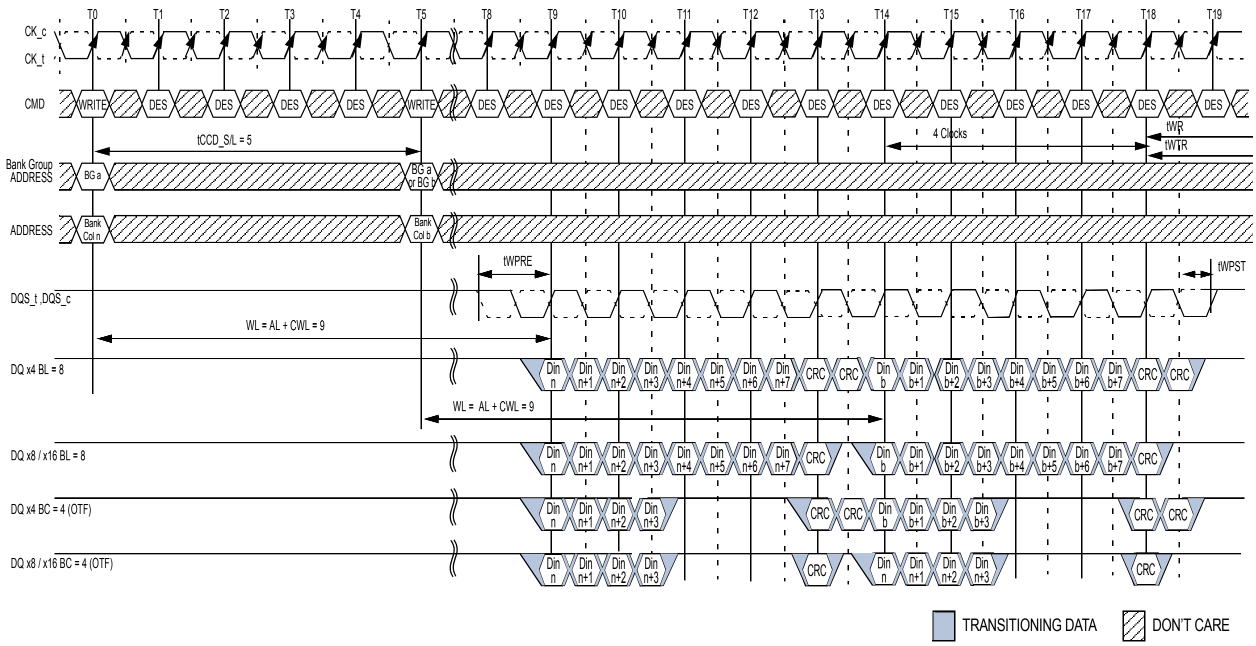
Figure 130. WRITE (BC4) Fixed with 1tCK Preamble and DBI



NOTE:

1. BL = 8, AL = 0, CWL = 9, PL = 4, Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T4.
5. CA Parity = Enable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

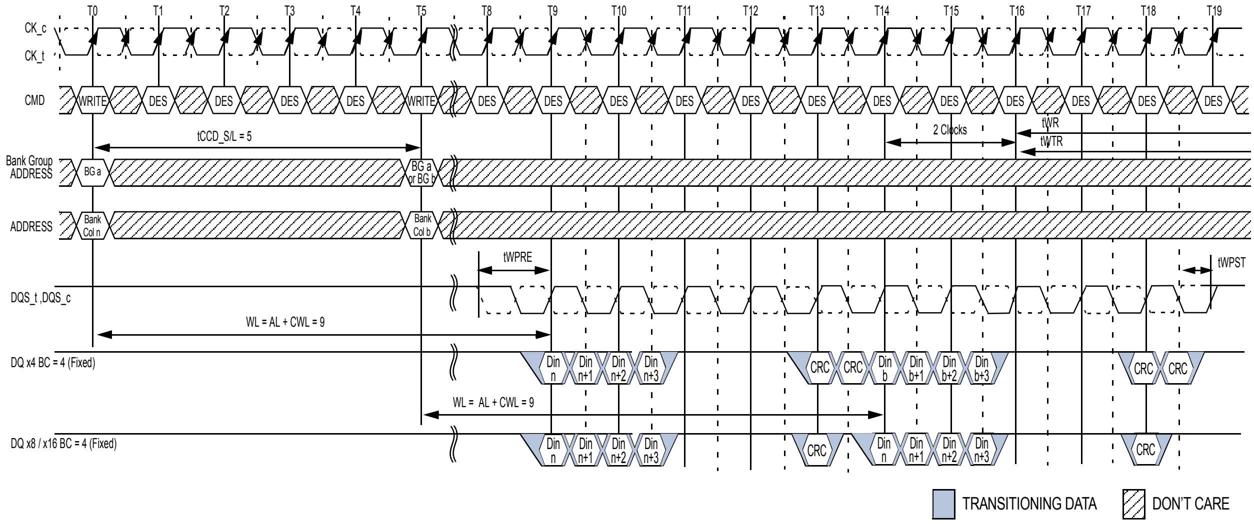
Figure 131. Consecutive WRITE (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE:

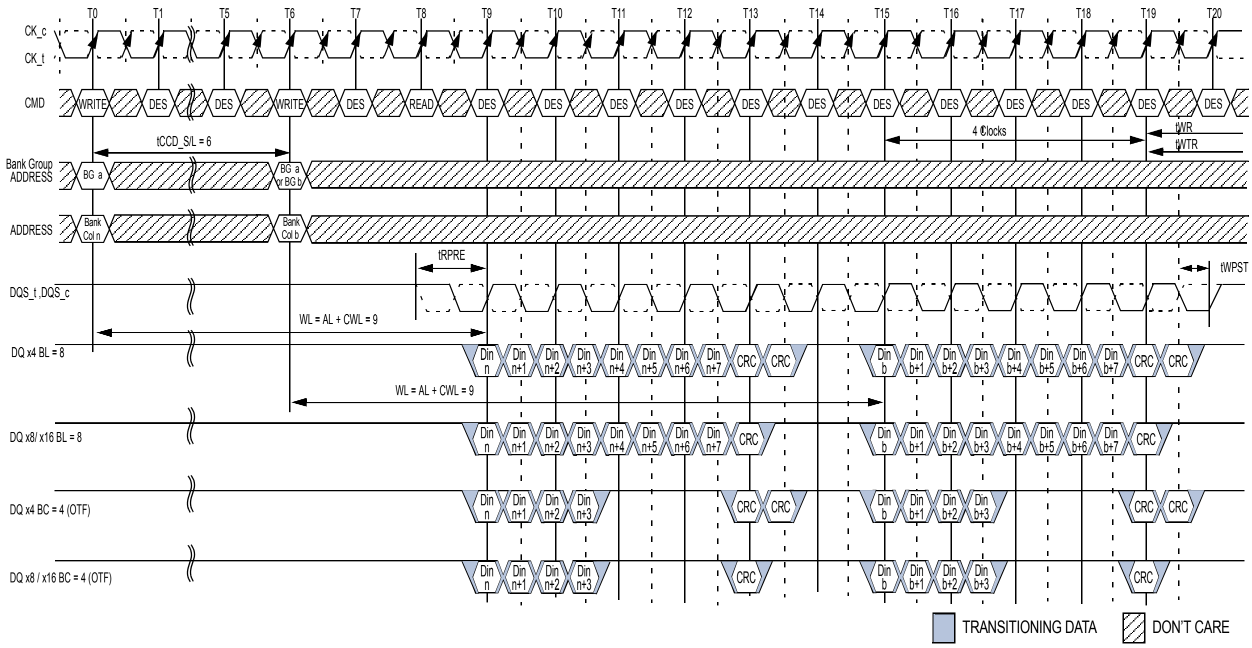
1. BL = 8/BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0 and T5.
5. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T5.
6. C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable, Write CRC = Enable.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18

Figure 132. Consecutive WRITE (BL8/BC4)OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



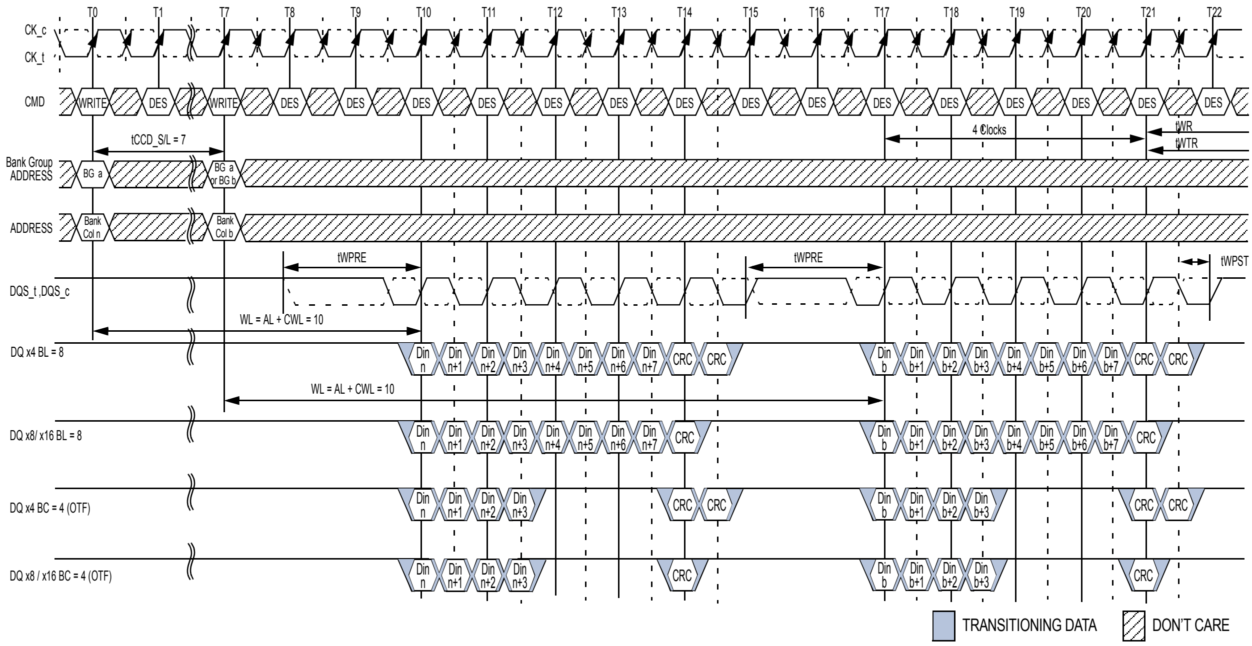
NOTE:
1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0] at T0 and T5.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T16.

Figure 133. Consecutive WRITE (BC4)Fixed with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE:
1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 6
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1A:0 = 0:0] or MR0[A1A:0 = 0:1] and A12 =1 during WRITE command at T0 and T6.
5. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0 and T6.
6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T19.

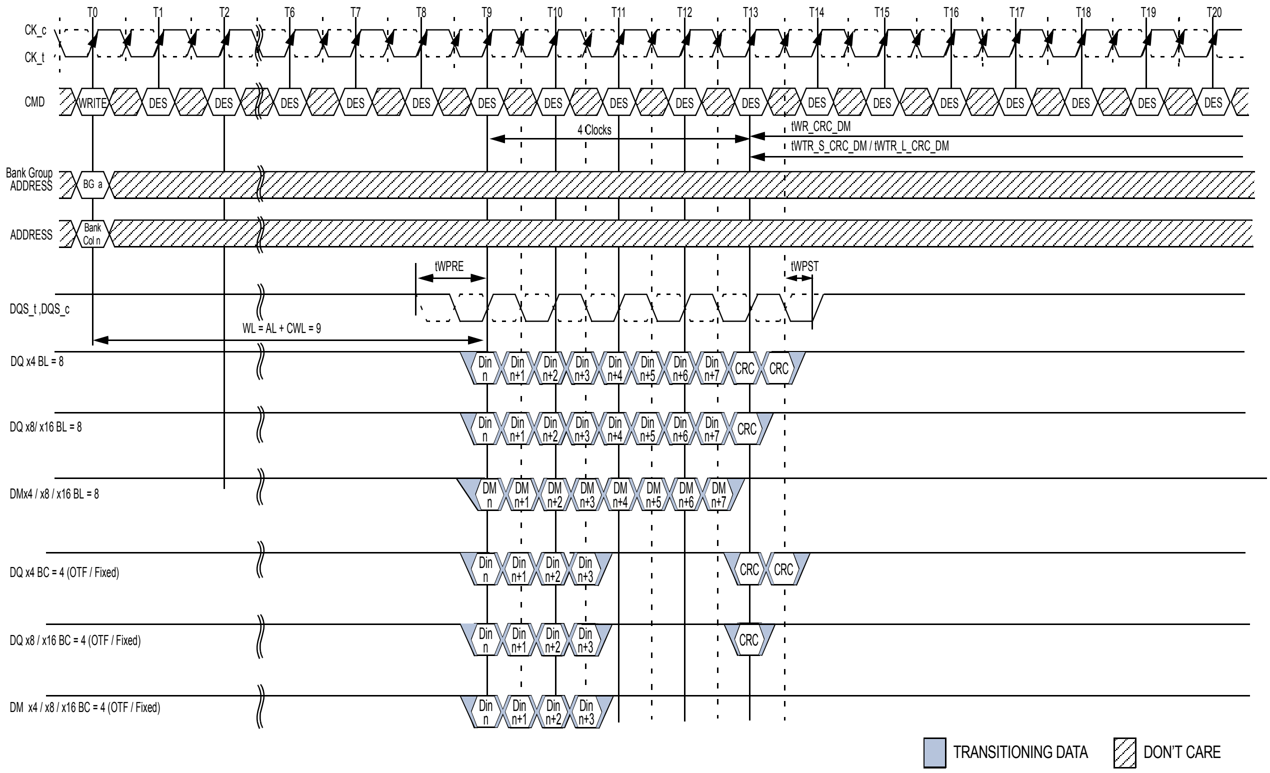
Figure 134. Nonconsecutive WRITE (BL8/BC4)OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE:

1. BL = 8, AL = 0, CWL = 9 + 1 = 10[9], Preamble = 2tCK, tCCD_S/L = 7
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T7.
5. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0 and T7.
6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.
7. tCCD_S/L = 6 isn't allowed in 2tCK preamble mode.
8. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.
9. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode

Figure 135. Nonconsecutive WRITE (BL8/BC4)OTF with 2tCK Preamble and Write CRC in Same or Different Bank Group



NOTE:

1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable, DM = Enable.
7. The write recovery time (tWR_CRC_ DM) and write timing parameter (tWR_S_CRC_ DM/tWR_L_CRC_ DM) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 136. WRITE (BL8/BC4)OTF/Fixed with 1tCK Preamble and Write CRC and DM in Same or Different Bank Group

2.25.6 Read and Write Command Interval

[Table 61] Minumum Read and Write Command Timings

Bank Group	Timing Parameter	DDR4-1600 / 1866 / 2133 / 2666 / 3200	Units	note
same	Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE		1, 2
	Minimum Read after Write	CWL + WBL / 2 + tWTR_L		1, 3
different	Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE		1, 2
	Minimum Read after Write	CWL + WBL / 2 + tWTR_S		1, 3

NOTE:
1. These timings require extended calibrations times tZQinit and tZQCS.
2. RBL : Read burst length associated with Read command
RBL = 8 for fixed 8 and on-the-fly mode 8
RBL = 4 for fixed BC4 and on-the-fly mode BC4
3. WBL : Write burst length associated with Write command
WBL = 8 for fixed 8 and on-the-fly mode 8 or BC4
WBL = 4 for fixed BC4 only

2.25.7 Write Timing Violations

2.25.7.1 Motivation

Generally, if Write timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable, for certain violations as specified below, the DRAM is guaranteed to not “hang up,” and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

2.25.7.2 Data Setup and Hold Offset Violations

Should the data to strobe timing requirements (Tdqs_off, Tdqh_off, Tdqs_dd_off, Tdqh_dd_off) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory locations addressed with this WRITE command.

In the example (Figure 112), the relevant strobe edges for write burst A are associated with the clock edges: T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5.

Subsequent reads from that location might results in unpredictable read data, however the DRAM will work properly otherwise.

2.25.7.3 Strobe and Strobe to Clock Timing Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise with the following constraints:

(1) Both Write CRC and data burst OTF are disabled; timing specifications other than tDQSH, tDQSL, tWPRE, tWPST, tDSS, tDSH, tDQSS are not violated.

(2) The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the Write-Latency position.

(3) A Read command following an offending Write command from any open bank is allowed.

(4) One or more subsequent WR or a subsequent WRA {to same bank as offending WR} may be issued tCCD_L later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending Writes. Reads from these Writes may provide incorrect data.

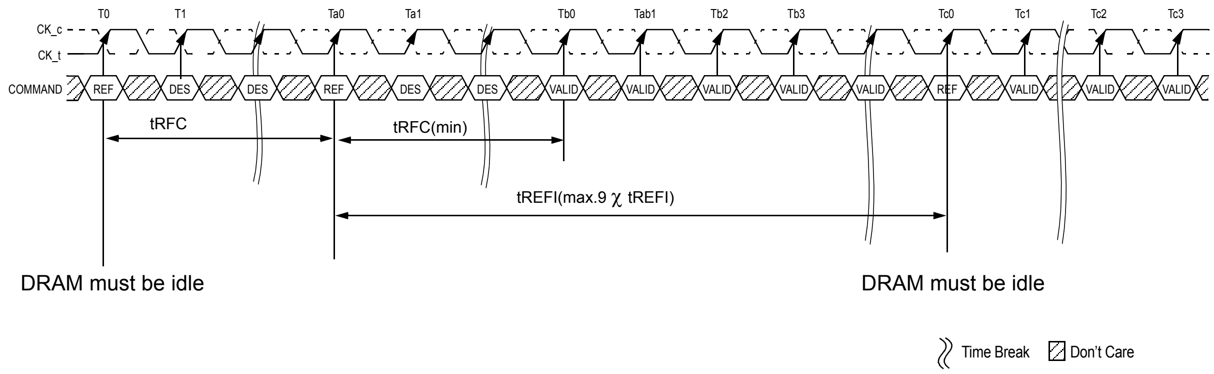
(5) One or more subsequent WR or a subsequent WRA {to a different bank group} may be issued tCCD_S later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending Writes. Reads from these Writes may provide incorrect data.

(6) Once one or more precharge commands(PRE or PREA) are issued to DDR4 after offending WRITE command and all banks become precharged state(idle state), a subsequent, non-offending WR or WRA to any open bank shall be able to write correct data.

2.26 Refresh Command

The Refresh command (REF) is used during normal operation of the DDR4 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR4 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When CS_n, RAS_n/A16 and CAS_n/A15 are held Low and WE_n/A14 and ACT_n are held High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don't Care” during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except DES, must be greater than or equal to the minimum Refresh cycle time tRFC(min) as shown in Figure X. Note that the tRFC timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the DDR4 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed when DRAM is in 1X refresh mode and for 2X/4X refresh mode, 16/32 Refresh commands can be postponed respectively during operation of the DDR4 SDRAM, meaning that at no point in time more than a total of 8,16,32 Refresh commands are allowed to be postponed for 1X,2X,4X Refresh mode respectively. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI (see Figure 137). In 2X and 4X Refresh mode, it's limited to 17 x tREFI2 and 33 x tREFI4. A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”) in 1X refresh mode and for 2X/4X refresh mode, 16/32 Refresh commands can be pulled in respectively, with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8/16/32, depending on Refresh mode, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI , 17 x tREFI2 and 33 x tREFI4 respectively. At any given time, a maximum of 16 REF/32REF 2/64REF 4 commands can be issued within 2 x tREFI/ 4 x tREFI2/ 8 x tREFI4



NOTE : 1. Only DES commands allowed after Refresh command registered untill tRFC(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 9 X tREFI.

Figure 137. Refresh Command Timing (Example of 1x Refresh mode)

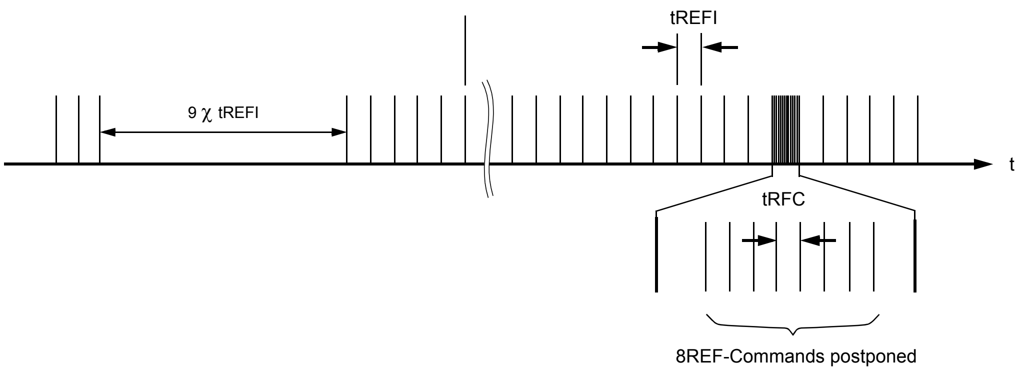


Figure 138. Postponing Refresh Commands (Example of 1X Refresh mode)

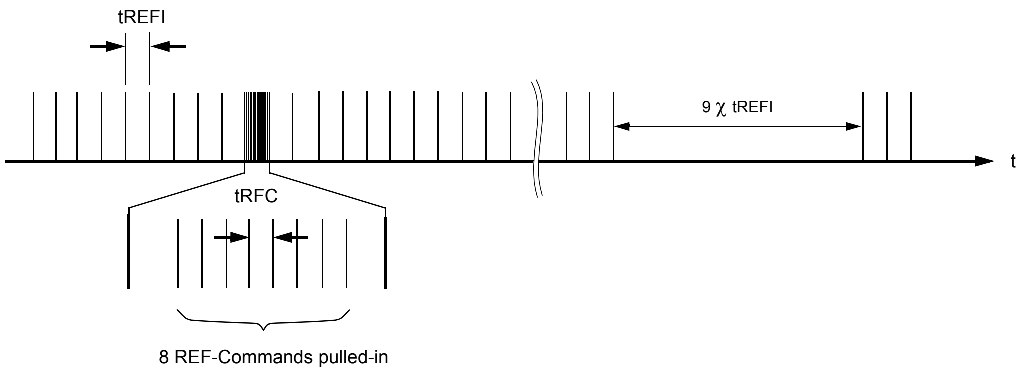


Figure 139. Pulling-in Refresh Commands (Example of 1X Refresh mode)

2.27 Self refresh Operation

The Self-Refresh command can be used to retain data in the DDR4 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR4 SDRAM retains data without external clocking.The DDR4 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS_n, RAS_n/A16, CAS_n/A15, and CKE held low with WE_n/A14 and ACT_n high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the DDR4 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD,tRFC, tZQinit, tZQoper, tZQCS, etc.). Deselect command must be registered on last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh Entry command is registered, Deselect command must also be registered at the next positive clock edge. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. .DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of ODT pin and RTT_PARK set when it enters in Self-Refresh mode. Upon exiting Self-Refresh, DRAM automatically enables ODT termination and set RTT_PARK asynchronously during tXSDLL when RTT_PARK is enabled. During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR4 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET_n, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VPP, and VRefCA) must be at valid levels. DRAM internal VrefDQ generator circuitry may remain ON or turned OFF depending on DRAM design. If DRAM internal VrefDQ circuitry is turned OFF in self refresh, when DRAM exits from self refresh state, it ensures that VrefDQ generator circuitry is powered up and stable within tXS period. First Write operation or first Write Leveling Activity may not occur earlier than tXS after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR4 SDRAM must remain in Self-Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.
The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and Deselect on command bus) is registered, following timing delay must be satisfied:

1. Commands that do not require locked DLL:
tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, tXSFast - ZQCL, ZQCS, MRS commands. For MRS command, only DRAM CL and WR/RTP register DLL Reset in MR0, RTT_NOM register in MR1, CWL and RTT_WR register in MR2 and geardown mode in MR3 Write and Read Preamble register in MR4, RTT_PARK register in MR5, tCCD_L/tDLLK and VrefDQ Training Value in MR6 are allowed to be accessed provided DRAM is not in per DRAM addressability mode. Access to other DRAM mode registers must satisfy tXS timing.
Note that synchronous ODT for write commands (WR, WRS4, WRS8, WRA, WRAS4 and WRAS8) and dynamic ODT controlled by write command require locked DLL.

2. Commands that require locked DLL:
tXSDLL - RD, RDS4, RDS8, RDA, RDAS4, RDAS8
Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in "ZQ Calibration Commands" on Section 2.12. To issue ZQ calibration commands, applicable timing requirements must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR4 SDRAM can be put back into Self-Refresh mode or Power down mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). Deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. Low level of ODT pin must be registered on each positive clock edge during tXSDLL when normal mode (DLL-on) is set. Under DLL-off mode, asynchronous ODT function might be allowed.
The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.

The exit timing from self-refresh exit to first valid command not requiring a locked DLL is tXS.
The value of tXS is (tRFC+10ns). This delay is to allow for any refreshes started by the DRAM to complete. tRFC continues to grow with higher density devices so tXS will grow as well.
A Bit A9 in MR4 is defined to enable the self refresh abort mode. If the bit is disabled then the controller uses tXS timings.
If the bit is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of tXS_abort.
Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

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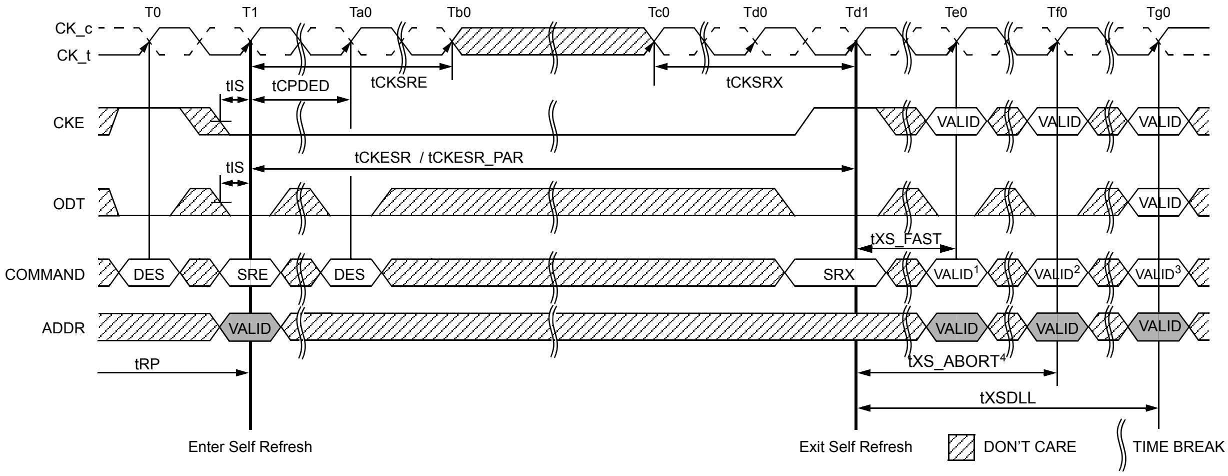


NOTE :
1. Only MRS (limited to those described in the Self-Refresh Operation section). ZQCS or ZQCL command allowed.
2. Valid commands not requiring a locked DLL
3. Valid commands requiring a locked DLL
4. Only DES is allowed during tXS_ABORT

Figure 140. Self-Refresh Entry/Exit Timing

2.27.1 Low Power Auto Self Refresh

DDR4 devices support Low Power Auto Self-Refresh (LP ASR) operation at multiple temperatures ranges (See temperature table below). Mode Register MR2 – descriptions

[Table 62] MR2 definitions for Low Power Auto Self-Refresh mode

A6	A7	Self-Refresh Operation Mode
0	0	Manual Mode – Normal operating temperature range
0	1	Manual Mode – Extended operating temperature range
1	0	Manual Mode – Lower power mode at a reduced operating temperature range
1	1	ASR Mode – automatically switching between all modes to optimize power for any of the temperature ranges listed above

Auto Self Refresh (ASR)
DDR4 DRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting the above MR2 bits A6=1 and A7=1. The DRAM will manage Self Refresh entry through the supported temperature range of the DRAM. In this mode, the DRAM will change self-refresh rate as the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

Manual Modes
If ASR mode is not enabled, the LP ASR Mode Register must be manually programmed to one the three self-refresh operating modes listed above. In this mode, the user has the flexibility to select a fixed self-refresh operating mode at the entry of the self-refresh according to their system memory temperature conditions. The user is responsible to maintain the required memory temperature condition for the mode selected during the self-refresh operation. The user may change the selected mode after exiting from self refresh and before the next self-refresh entry. If the temperature condition is exceeded for the mode selected, there is risk to data retention resulting in loss of data.

[Table 63] Self Refresh Function table

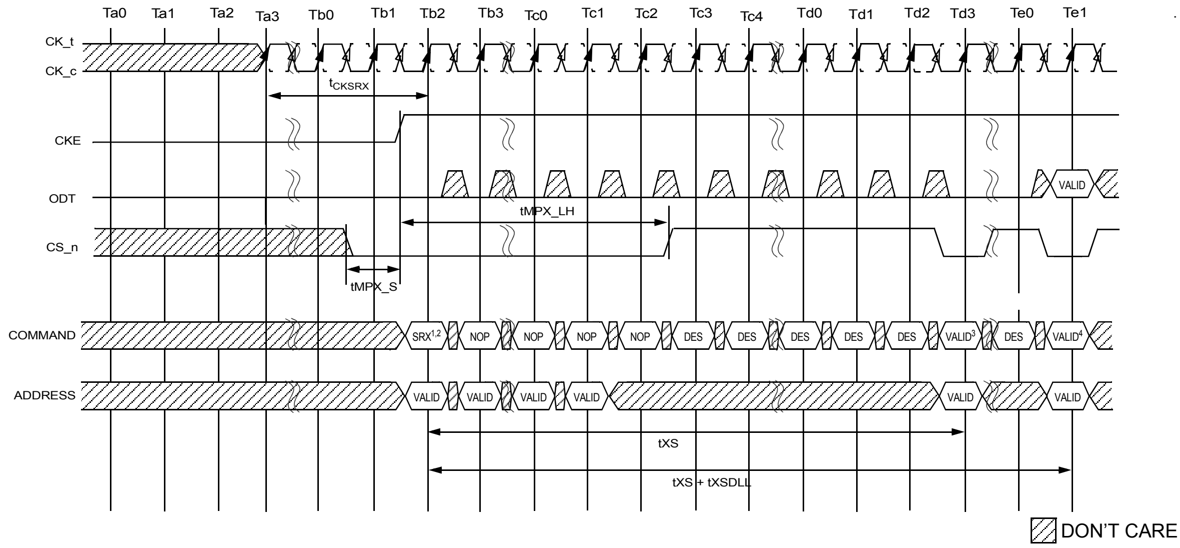
MR2-A6	MR2-A7	LP ASR Mode	Self Refresh Operation	Allowed Operating Temperature Range for Self Refresh Mode (all reference to DRAM Tcase)
0	0	Normal	Fixed normal self-Refresh rate to maintain data retention for the normal operating temperature. User is required to ensure 85°C DRAM Tcase-max is not exceeded to avoid any risk of data loss.	(0°C – 85°C)
0	1	Extended Temperature range	Fixed high self-Refresh rate to optimize data retention to support the extended temperature range	(0°C – 95°C)
1	0	Reduced Temperature range	Variable or fixed self-Refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM Tcasemax is not exceeded to avoid any risk of data loss .	(0°C – 45°C)
1	1	Auto Self Refresh	ASR Mode Enabled. Self-Refresh power consumption and data retention are optimized for any given operating temperature conditions	All of the above

2.27.2 Self Refresh Exit with No Operation command

Self Refresh Exit with No Operation command (NOP) allows for a common command/address bus between active DRAM and DRAM in Max Power Saving Mode. Self Refresh Mode may exit with No Operation commands (NOP) provided:

(1) The DRAM entered Self Refresh Mode with CA Parity and CAL disabled.
(2) tMPX_S and tMPX_LH are satisfied.
(3) NOP commands are only issued during tMPX_LH window.

No other command is allowed during tMPX_LH window after SRX command is issued.



NOTE :
1. CS_n = L, ACT_n = H, RAS_n/A16 = H, CAS_n/A15 = H, WE_n/A14 = H at Tb2 (No Operation command)
2. SRX at Tb2 is only allowed when DRAM shared Command/Address bus is under exiting Max Power Saving Mode.
3. Valid commands not requiring a locked DLL
4. Valid commands requiring a locked DLL
5. tXS_FAST and tXS_ABORT are not allowed this case.
6. Duration of CS_n Low around CKE rising edge must satisfy tMPX_S and tMPX_LH as defined by Max Power Saving Mode AC parameters.

Figure 141. Self Refresh Exit with No Operation command

2.28 Power down Mode

2.28.1 Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figure 143 through Figure 151 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, CKE and RESET_n. In power-down mode, DRAM ODT input buffer deactivation is based on MR5 bit A5. If it is configured to 0b, ODT input buffer remains on and ODT input signal must be at valid logic level. If it is configured to 1b, ODT input buffer is deactivated and DRAM ODT input signal may be floating and DRAM does not provide Rtt_Nom termination. Note that DRAM continues to provide Rtt_Park termination if it is enabled in DRAM mode register MR5 bit A8:A6 To protect DRAM internal delay on CKE line to block the input signals, multiple Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

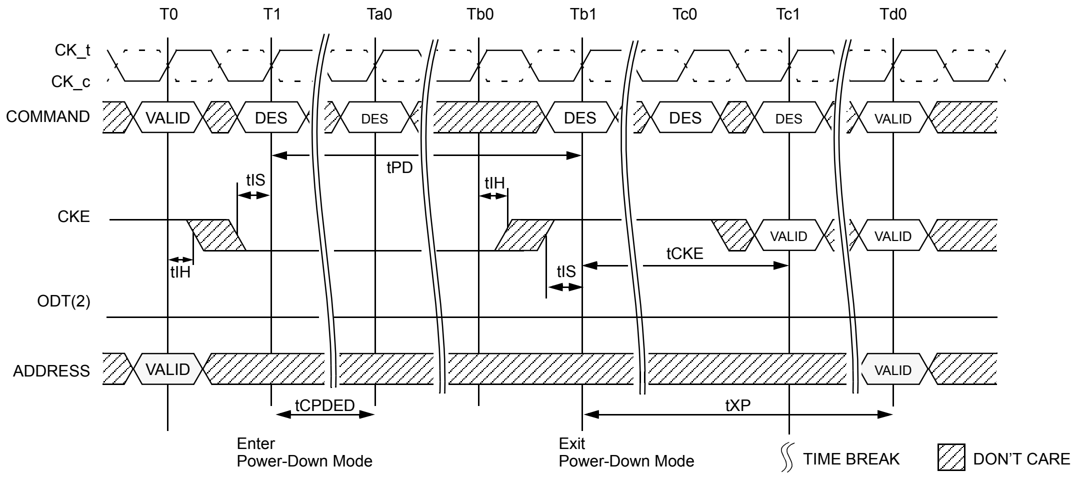
[Table 64] Power-Down Entry Definitions

Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	tXP to any valid command
Precharged (All banks Precharged)	On	Fast	tXP to any valid command.

Also, the DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE low, RESET_n high, and a stable clock signal must be maintained at the inputs of the DDR4 SDRAM, and ODT should be in a valid state, but all other input signals are “Don’t Care.” (If RESET_n goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

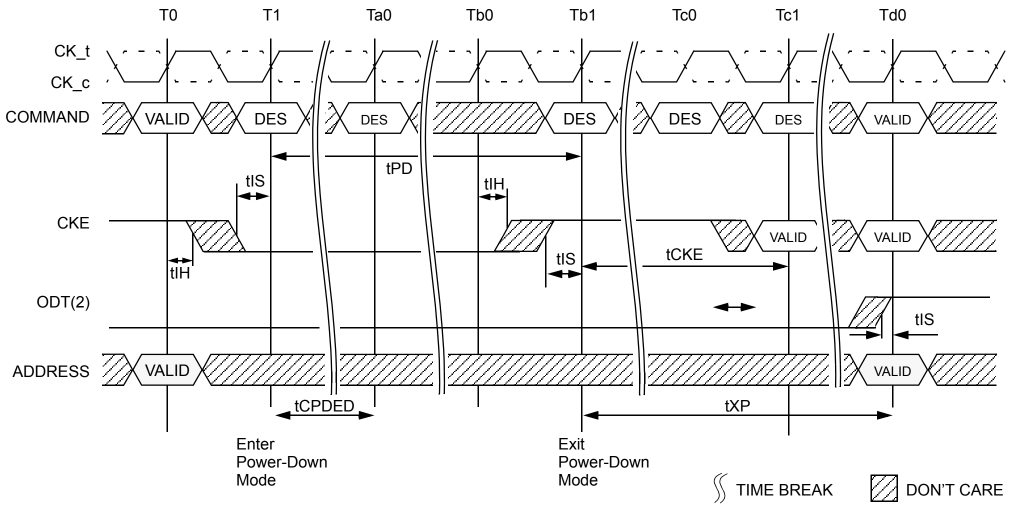
The power-down state is synchronously exited when CKE is registered high (along with a Deselect command). CKE high must be maintained until tCKE has been satisfied. DRAM ODT input signal must be at valid level when DRAM exits from power-down mode independent of MR5 bit A5 if Rtt_Nom is enabled in DRAM mode register. If DRAM Rtt_Nom is disabled then ODT input signal may remain floating. A valid, executable command can be applied with power-down exit latency, tXP after CKE goes high. Power-down exit latency is defined in the AC specifications table in Section 12.3.

Active Power Down Entry and Exit timing diagram example is shown in Figure 143. Timing Diagrams for CKE with PD Entry, PD Exit with Read and Read with Auto Precharge, Write, Write with Auto Precharge, Activate, Precharge, Refresh, and MRS are shown in Figure 144 through Figure 151. Additional clarification is shown in Figure 152.



NOTE : 1. VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.
2. ODT pin driven to a valid state. MR5 bit A5=0 (default setting) is shown.

Figure 142. Active Power-Down Entry and Exit Timing Diagram MR5 bit A5 =0



NOTE : 1. VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.
2. ODT pin driven to a valid state. MR5 bit A5=1 is shown.

Figure 143. Active Power-Down Entry and Exit Timing Diagram MR5 bit A5=1

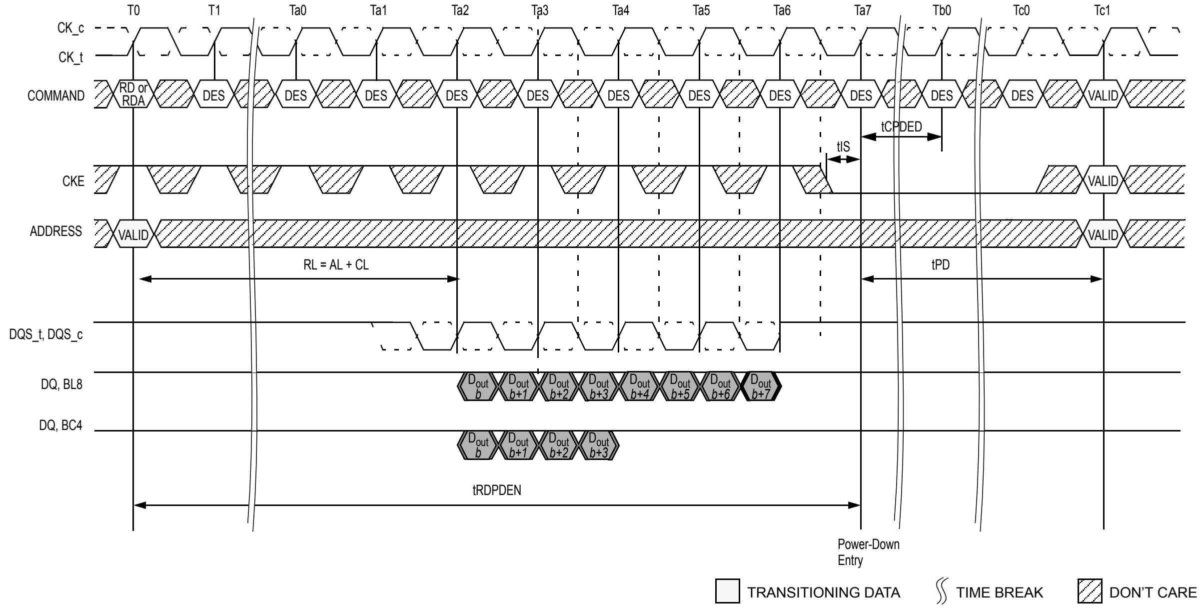
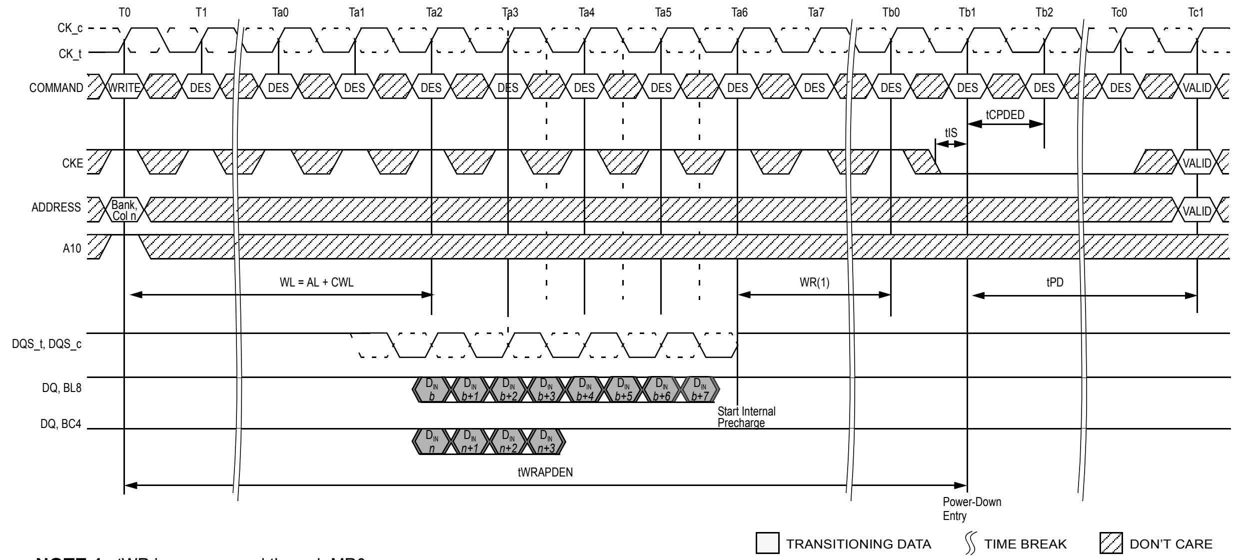


Figure 144. Power-Down Entry after Read and Read with Auto Precharge



NOTE 1. tWR is programmed through MR0.

Figure 145. Power-Down Entry After Write with Auto Precharge

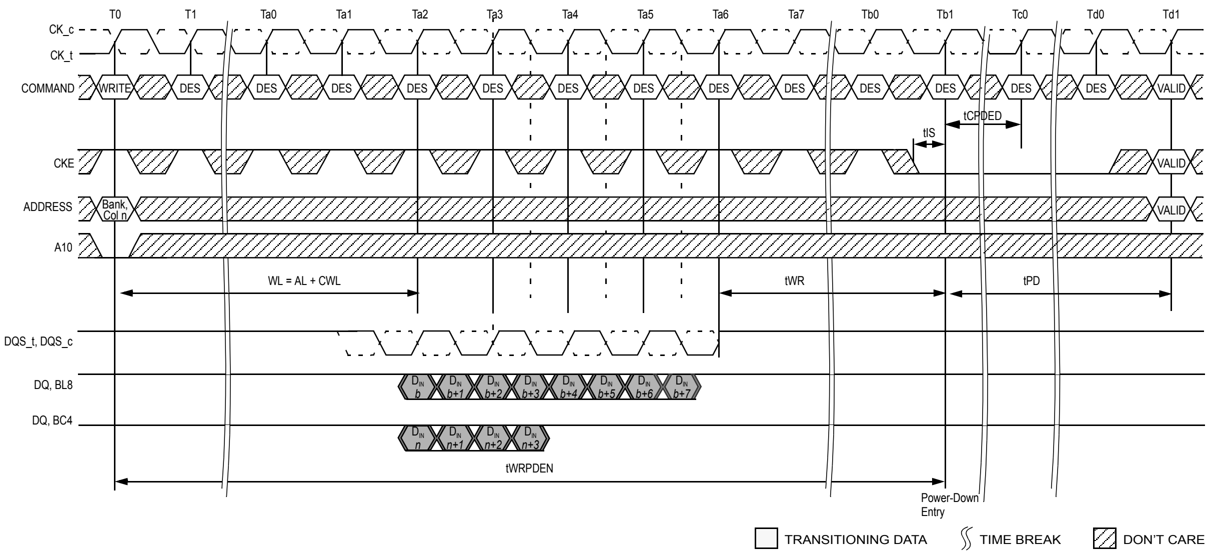


Figure 146. Power-Down Entry after Write

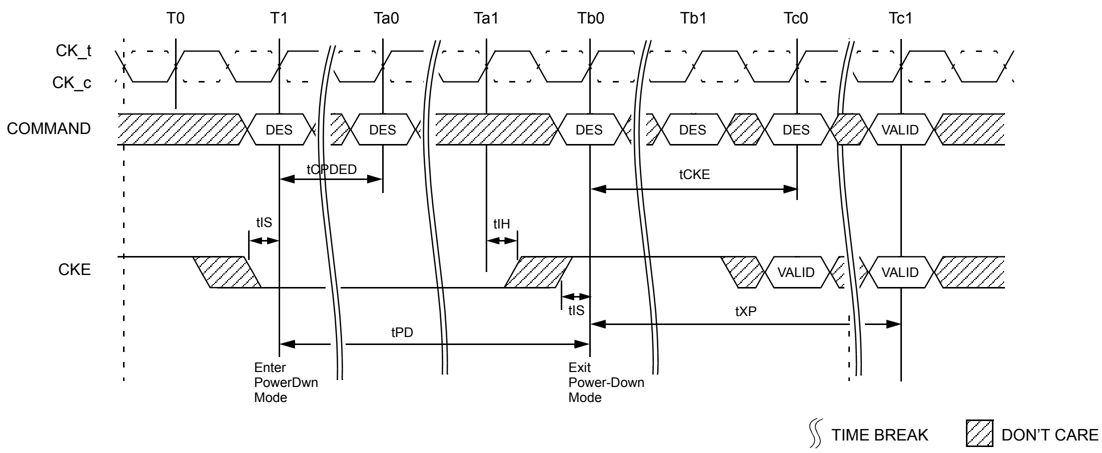


Figure 147. Precharge Power-Down Entry and Exit

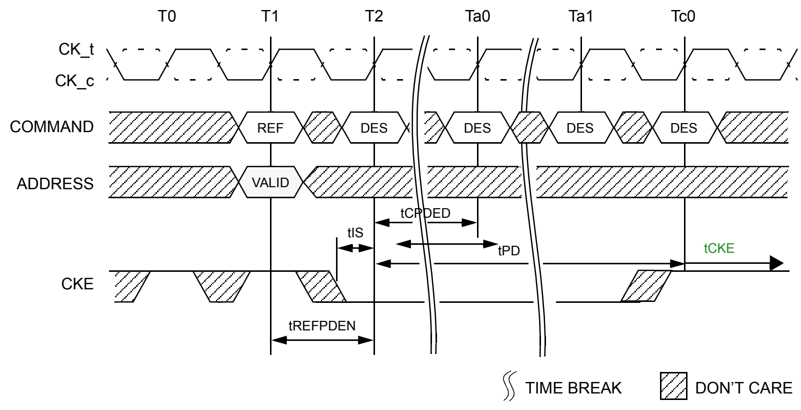


Figure 148. Refresh Command to Power-Down Entry

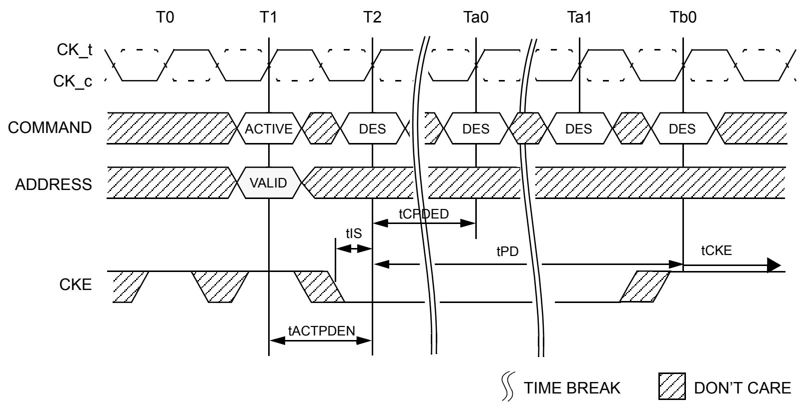


Figure 149. Activate Command to Power-Down Entry

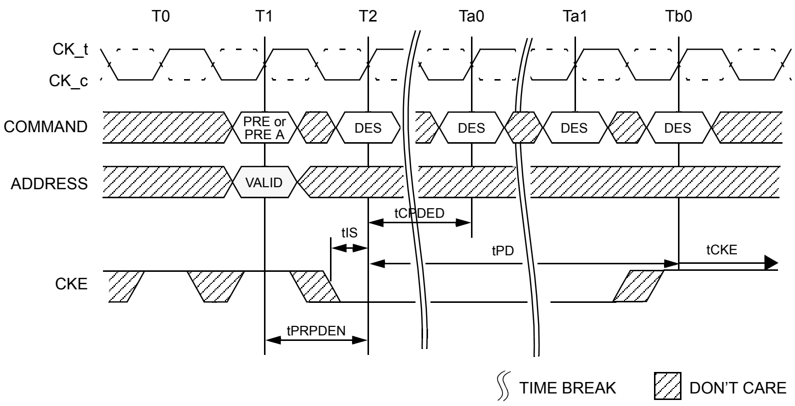


Figure 150. Precharge/Precharge all Command to Power-Down Entry

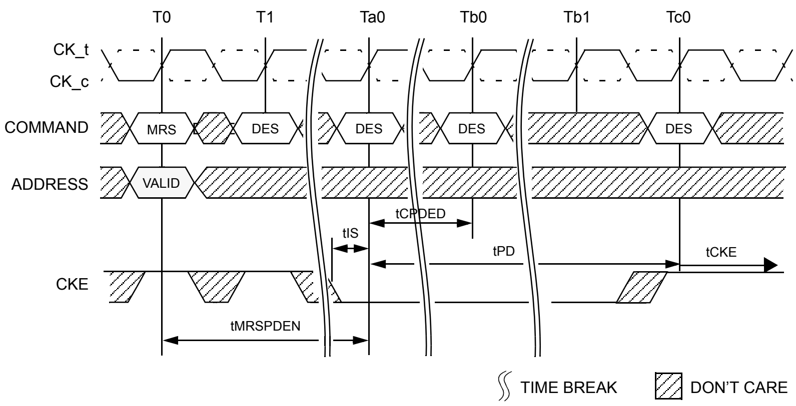


Figure 151. MRS Command to Power-Down Entry

2.28.2 Power-Down clarifications

When CKE is registered low for power-down entry, tPD(min) must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter tPD(min) is equal to the minimum value of parameter tCKE(min) as shown in Table "Timing Parameters by Speed Bin". A detailed example of Case1 is shown in Figure 152.

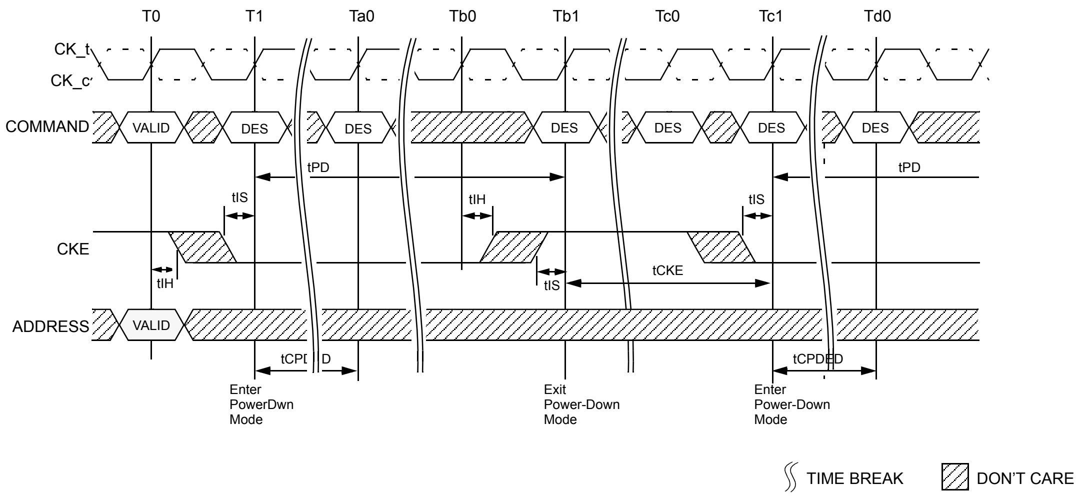


Figure 152. Power-Down Entry/Exit Clarification

2.28.3 Power Down Entry and Exit timing during Command/Address Parity Mode is Enable

Power Down entry and exit timing during Command/Address Parity mode is Enable are shown in Figure 153.

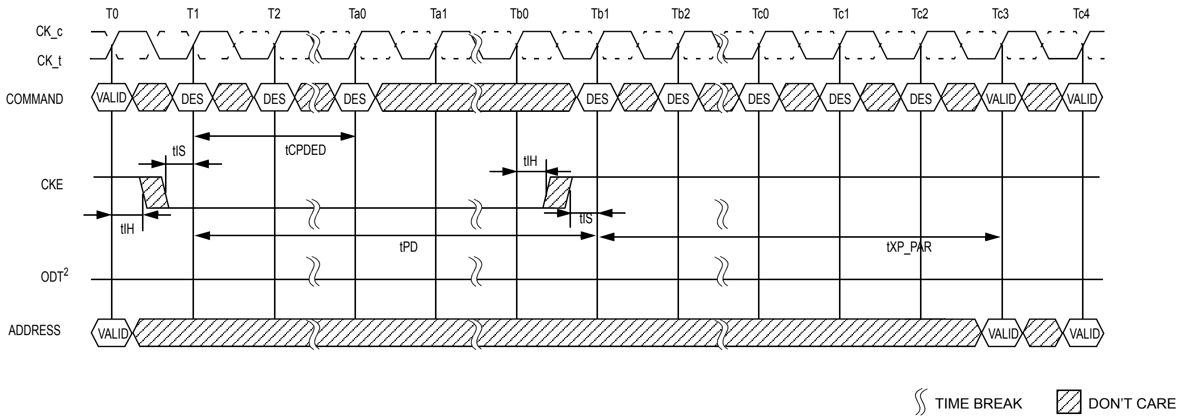


Figure 153. Power Down Entry and Exit Timing with C/A Parity

[Table 65] AC Timing Table

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled	tXP_PAR	max (4nCK,6ns) + PL	-	max (4nCK,6ns) + PL	-	max (4nCK,6ns) + PL	-	max (4nCK,6ns) + PL	-	

2.29 Maximum Power Saving Mode

2.29.1 Maximum power saving mode

This mode provides lowest power consuming mode which could be similar to the Self-Refresh status with no internal refresh activity. When DDR4 SDRAM is in the maximum power saving mode, it does not need to guarantee data retention nor respond to any external command (except maximum power saving mode exit and asserting RESET_n signal LOW) to minimize the power consumption.

2.29.2 Mode entry

Max power saving mode is entered through an MRS command. For devices with shared control/address signals, a single DRAM device can be entered into the max power saving mode using the per DRAM Addressability MRS command.
Note that large CS_n hold time to CKE upon the mode exit may cause DRAM malfunction, thus it is required that the CA parity, CAL and Gear Down modes are disabled prior to the max power saving mode entry MRS command.

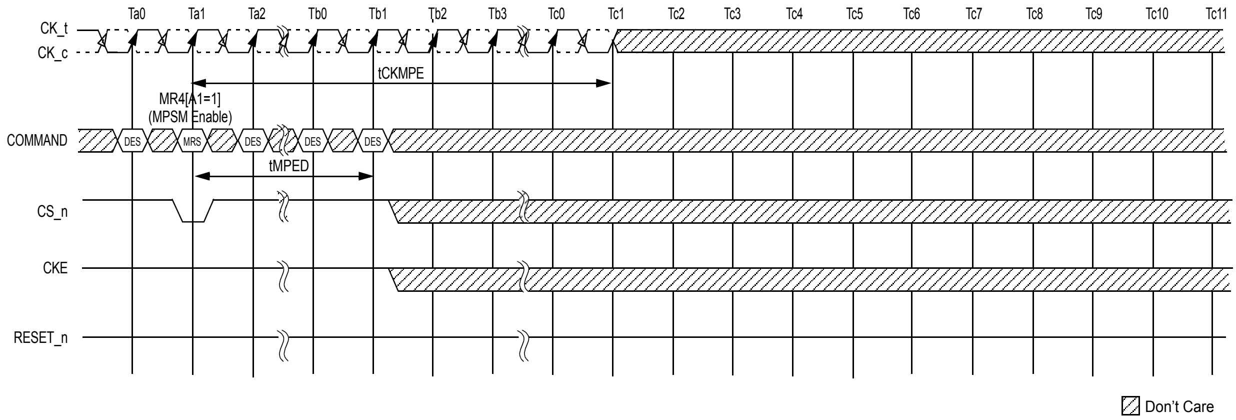


Figure 154. Maximum Power Saving mode Entry

Figure 155 below illustrates the sequence and timing parameters required for the maximum power saving mode with the per DRAM addressability (PDA).

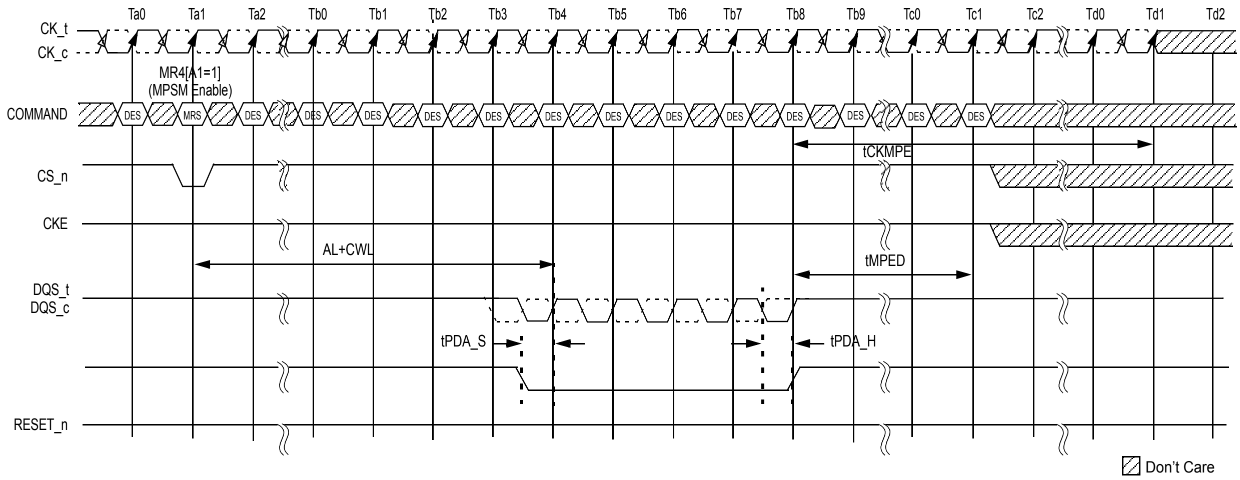


Figure 155. Maximum Power Saving mode Entry with PDA

When entering Maximum Power Saving mode, only DES commands are allowed until tMPED is satisfied. After tMPED period from the mode entry command, DRAM is not responsive to any input signals except CS_n, CKE and RESET_n signals, and all other input signals can be High-Z. CLK should be valid for tCKMPE period and then can be High-Z.

2.29.3 CKE transition during the mode

CKE toggle is allowed when DRAM is in the maximum power saving mode. To prevent the device from exiting the mode, CS_n should be issued 'High' at CKE 'L' to 'H' edge with appropriate setup tMPX_S and hold tMPX_HH timings.

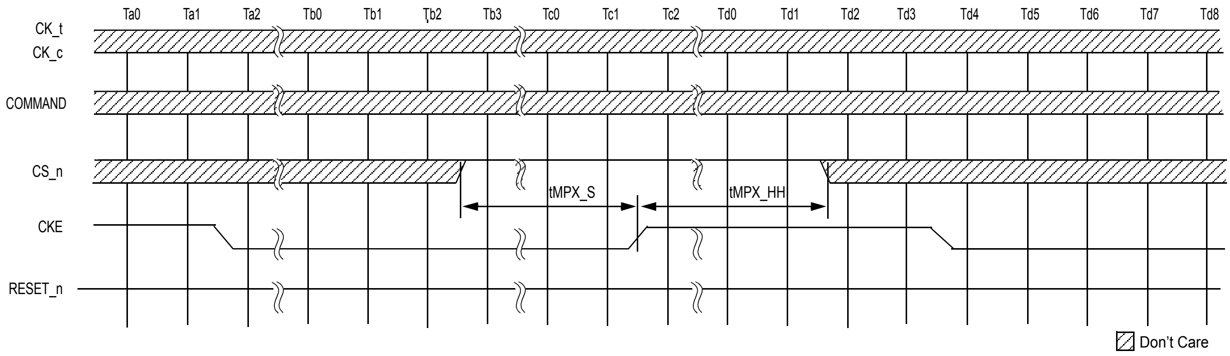


Figure 156. CKE Transition Limitation to hold Maximum Power Saving Mode

2.29.4 Mode exit

DRAM monitors CS_n signal level and when it detects CKE 'L' to 'H' transition, and either exits from the power saving mode or stay in the mode depending on the CS_n signal level at the CKE transition. Because CK receivers are shut down during this mode, CS_n = 'L' is captured by rising edge of the CKE signal. If CS_n signal level is detected 'L', then the DRAM initiates internal exit procedure from the power saving mode. CK must be restarted and stable tCKMPX period before the device can exit the maximum power saving mode. During the exit time tXMP, any valid commands except DES command is not allowed to DDR4 SDRAM and also tXMP_DLL, any valid commands requiring a locked DLL is not allowed to DDR4 SDRAM.

When recovering from this mode, the DRAM clears the MRS bits of this mode. It means that the setting of MR4 [A1] is move to '0' automatically.

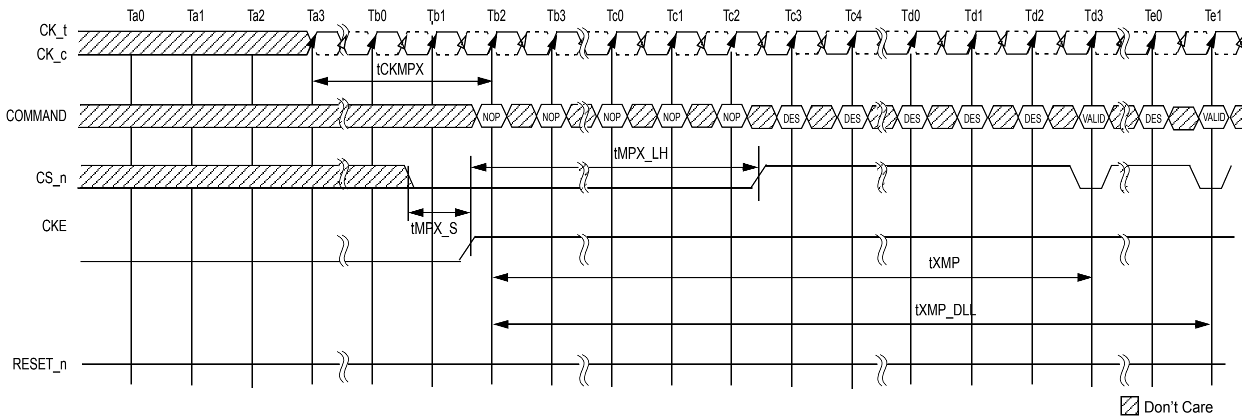


Figure 157. Maximum Power Saving Mode Exit Sequence

2.29.5 Timing parameter bin of Maximum Power Saving Mode for DDR4-1600/1866/2133/2400/2666/3200

Description	symbol	DDR4-1600/1866/2133/2400		DDR4-2666/3200		Unit	Note
		Min	Max	Min	Max		
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	TBD	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	TBD	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	TBD	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	TBD	-		
Exit MPSM to commands requir-ing a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	TBD	-		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	TBD	-		
CS_n High hold time to CKE rising edge	tMPX_HH	tXP(min)		TBD	-		
CS_n Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	TBD	TBD	ns	1

NOTE :
1. tMPX_LH(max) is defined with respect to actual tXMP in system as opposed to tXMP(min).

2.30 Connectivity Test Mode

2.30.1 Introduction

The DDR4 memory device supports a connectivity test (CT) mode, which is designed to greatly speed up testing of electrical continuity of pin interconnection on the PC boards between the DDR4 memory devices and the memory controller on the SoC. Designed to work seamlessly with any boundary scan devices, the CT mode is required for all x16 width devices independant of density and optional for all x8 and x4 width devices with densities greater than or equal to 8Gb.

Contrary to other conventional shift register based test mode, where test patterns are shifted in and out of the memory devices serially in each clock, DDR4's CT mode allows test patterns to be entered in parallel into the test input pins and the test results extracted in parallel from the test output pins of the DDR4 memory device at the same time, significantly enhancing the speed of the connectivity check. RESET_n is registered to High and VrefCA must be stable prior to entering CT mode. Once put in the CT mode, the DDR4 memory device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity check test results are available for extraction in parallel at the test output pins after a fixed propagation delay. During CT mode, any ODT is turned off.

A reset of the DDR4 memory device is required after exiting the CT mode.

2.30.2 Pin Mapping

Only digital pins can be tested via the CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the DDR4 memory device are classified as one of the following types:

1. Test Enable (TEN) pin: when asserted high, this pin causes the DDR4 memory device to enter the CT mode. In this mode, the normal memory function inside the DDR4 memory device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent ; additionally, the DRAM will set the internal VrefDQ to VDDQ*0.5 during CT mode (this is the only time the DRAM takes direct control over setting the internal VrefDQ). The TEN pin is dedicated to the connectivity check function and will not be used during normal memory operation.
2. Chip Select (CS_n) pin: when asserted low, this pin enables the test output pins in the DDR4 memory device. When de-asserted, the output pins in the DDR4 memory device will be tri-stated. The CS_n pin in the DDR4 memory device serves as the CS_n pin when in CT mode.
3. Test Input: a group of pins that are used during normal DDR4 DRAM operation are designated test input pins. These pins are used to enter the test pattern in CT mode.
4. Test Output: a group of pins that are used during normal DDR4 DRAM operation are designated test output pins. These pins are used for extraction of the connectivity test results in CT mode.
5. RESET_n : Fixed high level is required during CT mode same as normal function.

Table 59 below shows the pin classification of the DDR4 memory device.

[Table 66] Pin Classification of DDR4 Memory Device in Connectivity Test(CT) Mode

Pin Type in CT Mode		Pin Names during Normal Memory Operation
Test Enable		TEN
Chip Select		CS_n
Test Input	A	BA0-1, BG0-1, A0-A9, A10/AP, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, CKE, ACT_n, ODT, CLK_t, CLK_c, PAR
	B	DML_n/DBIL_n, DMU_n/DBIU_n, DM_n/DBI_n
	C	ALERT_n
	D	RESET_n
Test Output		DQ0 – DQ15, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DQS_t, DQS_c

[Table 67] Signal Description

Symbol	Type	Function
TEN	Input	Connectivity Test Mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation TEN is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e, 960mV for DC high and 240mV for DC low.

[Table 68] TEN Pin Weak Pull Down Strength Range

Symbol	Function	Min	Max	Unit
TEN	TEN pin should be internally pulled low to prevent DDR4 SDRAM from conducting Connectivity Test mode in case that TEN is not used. (Connectivity Test mode is required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb)	0.05	10	uA

NOTE: The host controller should use good enough strength when activating Connectivity Test mode to avoid current fighting at TEN signal and inability of Connectivity Test mode.

2.30.3 Logic Equations

2.30.3.1 Min Term Equations

MTx is an inernal signal to be used to generate the signal to drive the output signals.
x16 and x8 signals are internal signal indicating the density of the device.
MT0 = XOR (A1, A6, PAR)
MT1 = XOR (A8, ALERT_n, A9)
MT2 = XOR (A2, A5, A13)
MT3 = XOR (A0 A7, A11)
MT4 = XOR (CK_c, ODT, CAS_n/A15)
MT5 = XOR (CKE, RAS_n,/A16, A10/AP)
MT6 = XOR (ACT_n, A4, BA1)
MT7 = XOR (((x16 and DMU_n / DBIU_n) or (!x16 and BG1)), ((x8 or x16) and DML_n / DBIL_n), CK_t))
MT8 = XOR (WE_n / A14, A12 / BC, BA0)
MT9 = XOR (BG0, A3, (RESET_n and TEN))

2.30.3.2 Output equations for x16 devices

DQ0 = MT0
DQ1 = MT1
DQ2 = MT2
DQ3 = MT3
DQ4 = MT4
DQ5 = MT5
DQ6 = MT6
DQ7 = MT7
DQ8 = !DQ0
DQ9 = !DQ1
DQ10 = !DQ2
DQ11 = !DQ3
DQ12 = !DQ4
DQ13 = !DQ5
DQ14 = !DQ6
DQ15 = !DQ7
DQSL_t = MT8
DQSL_c = MT9
DQSU_t = !DQSL_t
DQSU_c = tDQSL_c

2.30.3.3 Output equations for x8 devices

DQ0 = MT0
DQ1 = MT1
DQ2 = MT2
DQ3 = MT3
DQ4 = MT4
DQ5 = MT5
DQ6 = MT6
DQ7 = MT7
DQS_t = MT8
DQS_c = MT9

2.30.3.4 Output equations for x4 devices

DQ0 = XOR(MT0, MT1)
DQ1 = XOR(MT2, MT3)
DQ2 = XOR(MT4, MT5)
DQ3 = XOR(MT6, MT7)
DQS_t = MT8
DQS_c = MT9

2.30.4 Input level and Timing Requirement

During CT Mode, input levels are defined below.
TEN pin : CMOS rail-to-rail with DC high and low at 80% and 20% of VDD.
CS_n : Pseudo differential signal referring to VrefCA
Test Input pin A : Pseudo differential signal referring to VrefCA
Test Input pin B : Pseudo differential signal referring to internal Vref 0.5*VDD
RESET_n : CMOS DC high above 70 % VDD
ALERT_n : Terminated to VDD. Swing level is TBD.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR4 memory device enter into the CT mode after tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on; once the DRAM is initialized and VREFdq is calibrated, CT Mode may no longer be used.

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR4 memory device are unknown and the integrity of the original content of the memory array is not guaranteed and therefore the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained High and Low respectively.

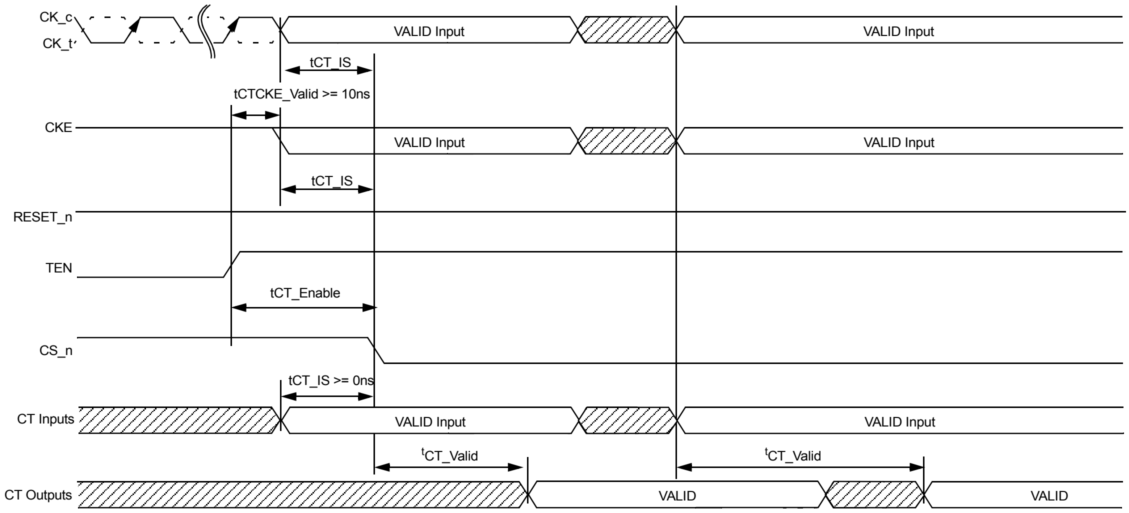


Figure 158. Timing Diagram for Connectivity Test(CT) Mode

[Table 69] AC parameters for Connectivity Test (CT) Mode

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

2.30.5 Connectivity Test (CT) Mode Input Levels

Following input parameters will be applied for DDR4 SDRAM Input Signal during Connectivity Test Mode.

[Table 70] CMOS rail to rail Input Levels for TEN

Parameter	Symbol	Min	Mix	Unit	Notes
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDD	VDD	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDD	VDD	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDD	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDD	V	2
TEN Input signal Falling time	TF_input_TEN	-	10	ns	
TEN Input signal Rising time	TR_input_TEN	-	10	ns	

NOTE:
1. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
2. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

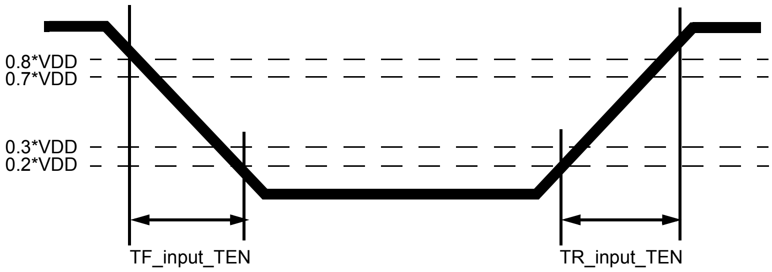


Figure 159. TEN Input Slew Rate Definition

[Table 71] Single-Ended AC and DC Input levels for CS_n, BA0-1, BG0-1,A0-A9, A10/AP, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, CKE, ACT_n, ODT, CLK_t, CLK_c, and PAR

Parameter	Symbol	Min	Mix	Unit	Notes
CTipA AC Input High Voltage	VIH(AC)_CTipA	VREFCA + 0.2	Note 1	V	
CTipA DC Input High Voltage	VIH(DC)_CTipA	VREFCA + 0.15	VDD	V	
CTipA DC Input Low Voltage	VIL(DC)_CTipA	VSS	VREFCA - 0.15	V	
CTipA AC Input Low Voltage	VIL(AC)_CTipA	Note 1	VREFCA - 0.2	V	
CTipA Input signal Falling time	TF_input_CTipA	-	5	ns	
CTipA Input signal Rising time	TR_input_CTipA	-	5	ns	

NOTE:
1 .See “Overshoot and Undershoot Specifications”.

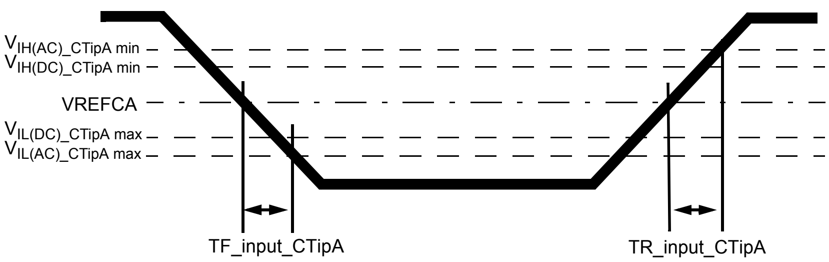


Figure 160. CS_n and Input A Slew Rate Definition

[Table 72] Single-Ended AC and DC Input levels for DML_n/DBIL_n, DMU_n/DBIU_n and DM_n/DBI_n

Parameter	Symbol	Min	Mix	Unit	Notes
CTipB AC Input High Voltage	VIH(AC)_CTipB	VREFDQ + 0.3	Note 2	V	1
CTipB DC Input High Voltage	VIH(DC)_CTipB	VREFDQ + 0.2	VDDQ	V	1
CTipB DC Input Low Voltage	VIL(DC)_CTipB	VSSQ	VREFDQ - 0.2	V	1
CTipB AC Input Low Voltage	VIL(AC)_CTipB	Note 2	VREFDQ - 0.3	V	1
CTipB Input signal Falling time	TF_input_CTipB	-	5	ns	
CTipB Input signal Rising time	TR_input_CTipB	-	5	ns	

NOTE:
1. VREFDQ is VDDQ*0.5
2 See "Overshoot and Undershoot Specifications"

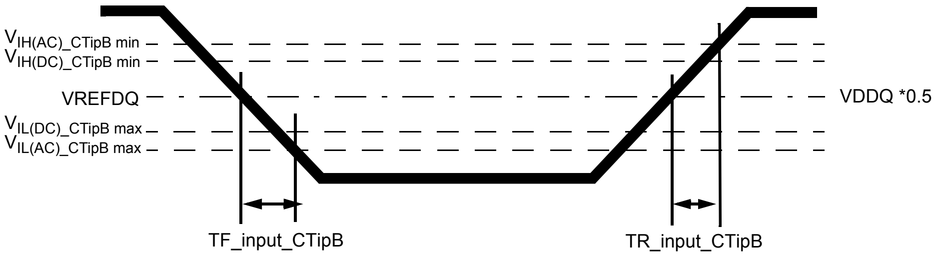


Figure 161. Input B Slew Rate Definition

2.30.5.1 Input Levels for RESET_n

RESET_n input condition is the same as normal operation, refer to Section 7.5.1.

2.30.5.2 Input Levels for ALERT_n

TBD

<Following table is just reference. >

[Table 73] Pin Classification of DDR4 Memory Device in Connectivity Test(CT) Mode

Pin Type in CT Mode		Pin Names during Normal Memory Operation
Test Enable		TEN
Chip Select		CS_n
Test Input	A	BA0-1, BG0-1, A0-A9, A10/AP, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, CKE, ACT_n, ODT, CLK_t, CLK_c, PAR
	B	DML_n/DBIL_n, DMU_n/DBIU_n, DM_n/DBI_n
	C	Alert_n
	D	RESET_n
Test Output		DQ0 – DQ15, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DQS_t, DQS_c

2.31 CLK to Read DQS timing parameters

DDR4 supports DLLOFF mode. Following parameters will be defined for CK to read DQS timings.

[Table 74] CLK to Read DQS Timing Parameters

Speed		DDR4-1600/1866/2133/2400/2666/3200			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**NOTE**
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	tDQSCK (DLL On)	refer to AC parameter tables	refer to AC parameter tables	ps	1, 3, 7, 8
	tDQSCK (DLL Off)	vendor specific	vendor specific	ps	2, 3, 7
DQS_t, DQS_c rising edge output variance window	tDQSCKi(DLL On)	-	refer to AC parameter tables	ps	1,5,6,7,8
	tDQSCKi(DLL Off)	-	TBD	ps	2,4,5,6,7
VDD sensitivity of tDQSCK (DLL Off)	dTDQSCKdV	-	TBD	ps/mV	2, 6
Temperature sensitivity of tDQSCK (DLL Off)	dTDQSCKdT	-	TBD	ps/^{o}C	2, 6

NOTE :

1 These parameters are applied when DRAM is in DLLON mode.
2 These parameters are applied when DRAM is in DLLOFF mode.
3 Measured over full VDD and Temperature spec ranges.
4 Measured at fixed and constant VDD and Temperature condition.
5 Measured for a given DRAM part, and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
6 These parameters are verified by design and characterization, and may not be subject to production test.
7 Assume no jitter on input clock signals to the DRAM.
8 Refer to Section 2.24.1 READ Timing Definitions.

DQSCK(DLL On),Min limit = Earliset of {tDQSCKi(DLL On) , at any valid VDD and Temperature , all DQS pairs and parts}
tDQSCK(DLL On),Max limit = Latest of {tDQSCKi(DLL On) , at any valid VDD and Temperature , all DQS pairs and parts}
tDQSCK(DLL Off),Min limit = Earliset of {tDQSCKi(DLL Off), at any valid VDD and Temperature, all DQS pairs and parts}
tDQSCK(DLL Off),Max limit = Latest of {tDQSCKi(DLL Off), at any valid VDD and Temperature, all DQS pairs and parts}

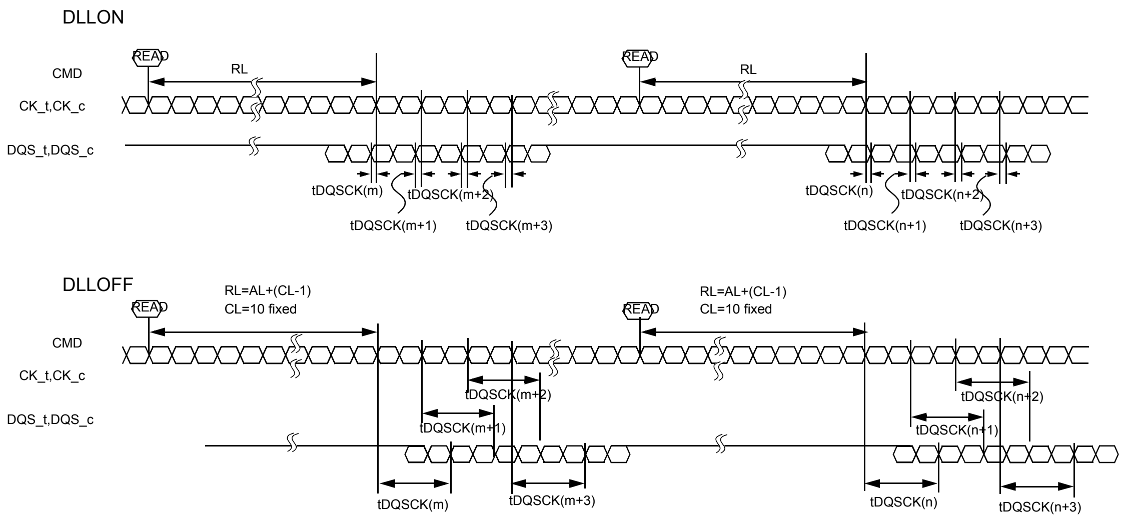
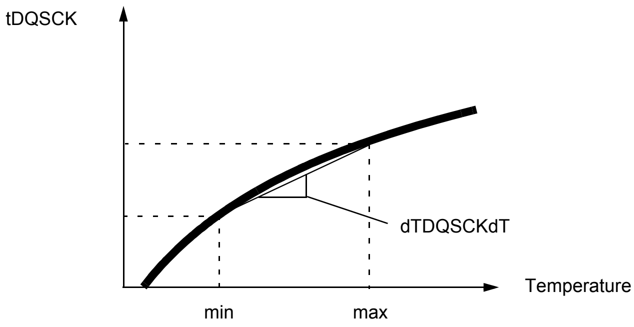
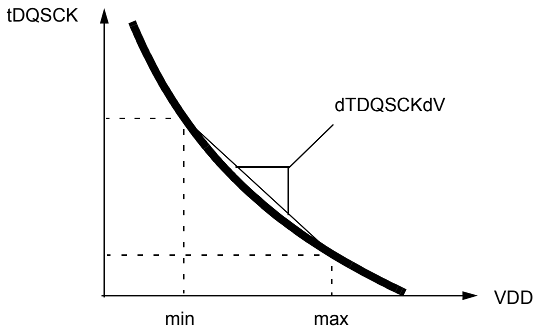


Figure 162. tDQSCK Definition Difference between DLL ON and DLL OFF



dTDQSCKdT = l tDQSCK(Toper,max) - tDQSCK(Toper,min)l / lToper,max - Toper,minl

Figure 163. dTDQSCKTdT Definition



dTDQSCKdV = l tDQSCK(VDD,max) - tDQSCK(VDD,min)l / lVDD,max - VDD,minl

Figure 164. TDQSCKTdV Definition

2.32 Post Package Repair (PPR)

DDR4 supports Fail Row address repair as optional feature for 4Gb and required for 8Gb and above. Supporting PPR is identified via Datasheet and SPD in Module so should refer to DRAM manufacturer’s Datasheet. PPR provides simple and easy repair method in the system and Fail Row address can be repaired by the electrical programming of Electrical-fuse scheme.

With PPR, DDR4 can correct 1Row per Bank Group

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the PPR mode entry and repair. (i.e. Command/Address training period)

DDR4 defines two fail row address repair sequences and users can choose to use among those 2 command sequences.
First command sequence is to use WRA command and ensure data retention with Refresh operation except for the bank containing row that is being repaired. Second command sequence is to use WR command and Refresh operation can’t be performed in the sequence. So, the second command sequence doesn’t ensure data retention for target DRAM.

2.32.1 DDR4 Post Package Repair Guard Key

Entry into PPR is protected through a sequential MRS guard key to prevent unintentional programming. The key is entered as a string of four MR0 commands after MR4 bit 13 is set to “1” to enable PPR mode. The string of four MR0 commands must be entered in order as specified in the spec. Any Interruption of the key sequence with other MR commands and other commands such as ACT, WR, RD, PRE, REF, ZQ, NOP, RFU is not allowed. If the MR0 bits are not entered in the required order or interrupted with other MR commands, PPR will not be enabled, the programming cycle will result in a no-op. And when PPR entry sequence is interrupted, followed up ACT and WR commands will be conducted as normal DRAM commands. No error indication is given if an incorrect code is entered other than the programming cycle will not occur. To restart the PPR if the sequence is interrupted, the MR4 bit 13 must be cleared and re-set.

2.32.1.1 Post Package Repair of a Fail Row Address

The following is the enable procedure of PPR.
1. Before entering „PPR“ mode, all banks must be Precharged; DBI and CRC Modes must be disabled
2. Enable PPR using MR4 bit “A13=1” and wait tMOD
3. Issue guard Key as four consecutive MR0 commands each with a unique address field A[17:0]. Each MR0 command should space by tMOD
4. Issue ACT command with the Bank and Row Fail address, Write data is used to select the individual DRAM in the Rank for repair.
The rest of the PPR command is unchanged.

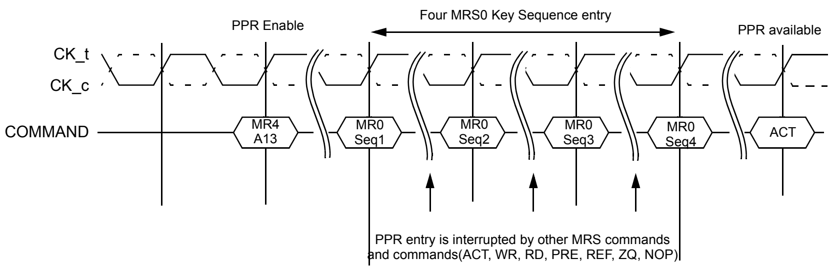


Figure 165. Timing Diagram for soft PPR Key Sequence

[Table 75] MR0 Key Sequence (Option 1)

Guard Keys	BG1:0	BA1:0	A17:12	A11	A10	A9	A8	A7	A6:0
1ST MR0	0	0	x	1	1	0	0	1	1
2ST MR0	0	0	x	0	1	1	1	1	1
3ST MR0	0	0	x	1	0	1	1	1	1
4ST MR0	0	0	x	0	0	1	1	1	1

[Table 76] MR0 Key Sequence (Option 2)

Guard Keys	BG1:0	BA1:0	A17:12	A11	A10	A9	A8	A7	A6:0
1ST MR0	0	0	x	1	1	0	0	1	x

2ST MR0	0	0	x	0	1	1	1	1	x
3ST MR0	0	0	x	1	0	1	1	1	x
4ST MR0	0	0	x	0	0	1	1	1	x

Note: There are two options for MR0 key sequence and it's dependent on vendor's implementation as in Table 68 & Table 69 Option 1 in table 1 is allowed in all DDR4 density but option 2 in Table 69 is only allowed in 4Gb & 8Gb DDR4 product. Please refer to vendor datasheet regarding MR0 key sequence.

2.32.2 Fail Row Address Repair (WRA case)

The following is procedure of PPR with WRA command.

1. Before entering 'PPR' mode, All banks must be Precharged; DBI and CRC Modes must be disabled
2. Enable PPR using MR4 bit "A13=1" and wait tMOD
3. Issue ACT command with Fail Row address
4. After tRCD, Issue WRA with VALID address. DRAM will consider Valid address with WRA command as 'Don't Care'
5. After WL(WL=CWL+AL+PL), All DQs of Target DRAM should be LOW for 4tCK. If HIGH is driven to All DQs of a DRAM consecutively for equal to or longer than 2tCK, then DRAM does not conduct PPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4tCK nor HIGH for equal to or longer than 2tCK , then PPR mode execution is unknown.
6. Wait tPGM to allow DRAM repair target Row Address internally and issue PRE
7. Wait tPGM_Exit after PRE which allow DRAM to recognize repaired Row address
8. Exit PPR with setting MR4 bit "A13=0"
9. DDR4 will accept any valid command after tPGMPST
10. In More than one fail address repair case, Repeat Step 2 to 9

In addition to that, PPR mode allows REF commands from PL+WL+BL/2+tWR+tRP after WRA command during tPGM and tPGMPST for proper repair; provided multiple REF commands are issued at a rate of tREFI or tREFI/2, however back-to-back REF commands must be separated by at least tREFI/4 when the DRAM is in PPR mode. Upon receiving REF command, DRAM performs normal Refresh operation and maintains the array content except for the Bank containing row that is being repaired. Other command except REF during tPGM can cause incomplete repair so no other command except REF is allowed during tPGM

Once PPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after PPR exit with MR4 [A13=0] and tPGMPST

2.32.3 Fail Row Address Repair (WR case)

The following is procedure of PPR with WR command.

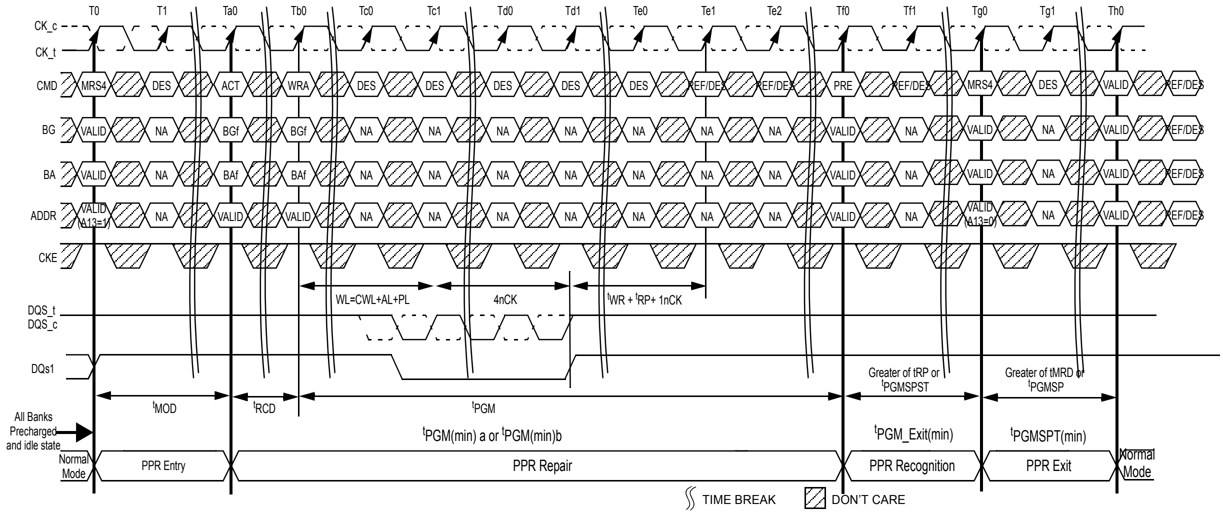
1. Before entering 'PPR' mode, All banks must be Precharged; DBI and CRC Modes must be disabled
2. Enable PPR using MR4 bit "A13=1" and wait tMOD
3. Issue ACT command with Fail Row address
4. After tRCD, Issue WR with VALID address. DRAM will consider Valid address with WR command as 'Don't Care'
5. After WL(WL=CWL+AL+PL), All DQs of Target DRAM should be LOW for 4tCK. If HIGH is driven to All DQs of a DRAM consecutively for equal to or longer than 2tCK, then DRAM does not conduct PPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4tCK nor HIGH for equal to or longer than 2tCK , then PPR mode execution is unknown.
6. Wait tPGM to allow DRAM repair target Row Address internally and issue PRE
7. Wait tPGM_Exit after PRE which allow DRAM to recognize repaired Row address
8. Exit PPR with setting MR4 bit "A13=0"
9. DDR4 will accept any valid command after tPGMPST
10. In More than one fail address repair case, Repeat Step 2 to 9

In this sequence, Refresh command is not allowed between PPR MRS entry and exit.

Once PPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after PPR exit with MR4 [A13=0] and tPGMPST

[Table 77] PPR Setting

MR4 [A13]	Description
0	PPR Disabled
1	PPR Enabled



Note
1. Allow REF(1X) from PL+WL+BL/2+tWR+tRP after WR
2. Timing diagram shows possible commands but not all shown can be issued at same time; for example if REF is issued at Te1, DES must be issued at Te2 as REF would be illegal at Te2. Likewise, DES must be issued tRFC prior to PRE at Tf0. All regular timings must still be satisfied.

Figure 166. Fail Row Repair (WRA Case)

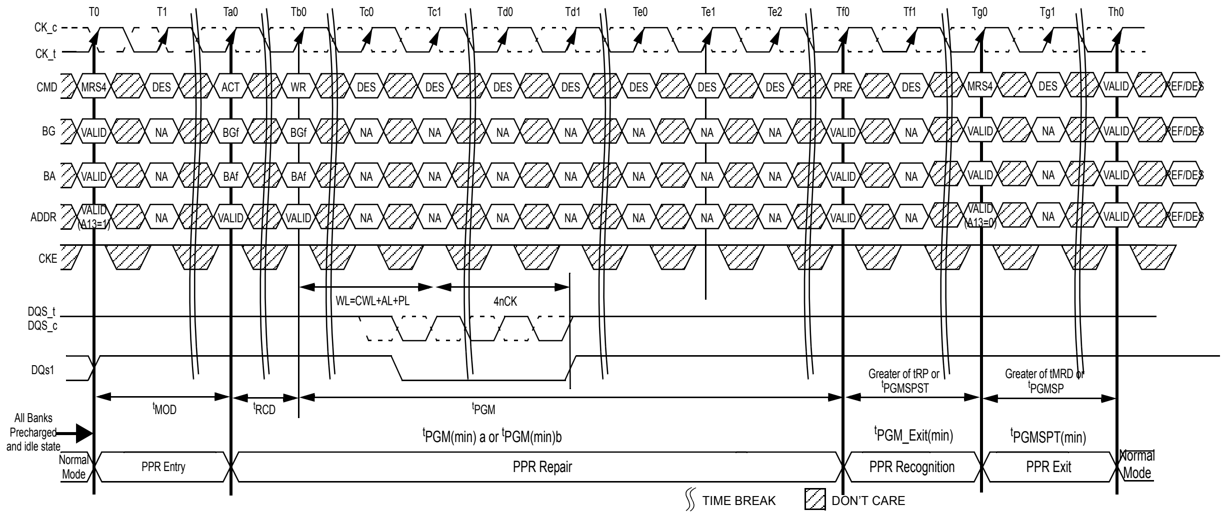


Figure 167. Fail Row Repair (WR Case)

2.32.4 Programming PPR support in MPR0 page2

PPR is optional feature of DDR4 4Gb so Host can recognize if DRAM is supporting PPR or not by reading out MPR0 Page2.
MPR page2;
PPR is supported : [7]=1
PPR is not supported : [7]=0
soft PPR is supported : [6]=1
soft PPR is not supported : [6]=0

[Table 78] Number of Repairable Row

<table>
<tr><th>Address</th><th>MPR Location</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>note</th></tr>
<tr><td rowspan="12">BA1:BA0</td><td rowspan="3">00 = MPR0</td><td>PPR</td><td>sPPR</td><td>RFU</td><td colspan="2">Temperature Sensor Status(Table1)</td><td>CRC Write Enable</td><td colspan="2">Rtt_WR</td><td rowspan="12">read-only</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>MR2</td><td colspan="2">MR2</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A12</td><td>A10</td><td>A9</td></tr>
<tr><td rowspan="3">01= MPR1</td><td>Vref DQ Trng range</td><td colspan="6">Vref DQ training Value</td><td>Gear-down Enable</td></tr>
<tr><td>MR6</td><td colspan="6">MR6</td><td>MR3</td></tr>
<tr><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>A3</td></tr>
<tr><td rowspan="3">10 = MPR2</td><td colspan="4">CAS Latency</td><td>RFU</td><td colspan="3">CAS Write Latency</td></tr>
<tr><td colspan="4">MR0</td><td>-</td><td colspan="3">MR2</td></tr>
<tr><td>A6</td><td>A5</td><td>A4</td><td>A2</td><td>-</td><td>A5</td><td>A4</td><td>A3</td></tr>
<tr><td rowspan="3">11 = MPR3</td><td colspan="3">Rtt_Nom</td><td colspan="3">Rtt_Park</td><td colspan="2">Driver Impedance</td></tr>
<tr><td colspan="3">MR1</td><td colspan="3">MR5</td><td colspan="2">MR2</td></tr>
<tr><td>A10</td><td>A9</td><td>A6</td><td>A8</td><td>A7</td><td>A6</td><td>A2</td><td>A1</td></tr>
</table>

2.32.5 Required Timing Parameters

Repair requires additional time period to repair Fail Row Address into spare Row address and the followings are requirement timing parameters for PPR

[Table 79] PPR Timing Parameters

<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">DDR4-1600/1866/2133/2400</th><th colspan="2">DDR4-2666/3200</th><th rowspan="2">Unit</th><th rowspan="2">Note</th></tr>
<tr><th>min</th><th>max</th><th>min</th><th>max</th></tr>
<tr><td>PPR Programming Time: x4/x8</td><td>tPGMa</td><td>1,000</td><td>-</td><td>1,000</td><td>-</td><td>ms</td><td></td></tr>
<tr><td>PPR Programming Time: x16</td><td>tPGMb</td><td>2,000</td><td>-</td><td>2,000</td><td>-</td><td>ms</td><td></td></tr>
<tr><td>PPR Exit Time</td><td>tPGM_Exit</td><td>15</td><td>-</td><td>15</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>New Address Setting time</td><td>tPGMPST</td><td>50</td><td>-</td><td>50</td><td>-</td><td>us</td><td></td></tr>
</table>

2.33 Soft Post Package Repair (sPPR)

Soft Post Package Repair (sPPR) is a way to quickly, but temporarily, repair a row element in a Bank Group on a DDR4 DRAM device, contrasted to hard Post Package Repair which takes longer but is permanent repair of a row element. There are some limitations and differences between Soft Repair and a Hard Repair

	Soft Repair	**Hard Repair**	**Note**
Persistence of Repair	Volatile – Repaired as long as VDD is within Operating Range	Non-Volatile – repair is permanent after the repair cycle.	Soft Repair erased when Vdd removed or device reset.
Length of time to complete repair cycle	tWR	>200ms	
# of Repair elements	Only 1 per BG	1 per BG	A subsequent sPPR can be performed without affecting the PPR previously performed provided a row is available in that bank group
Simultaneous use of soft and hard repair within a BG	Previous hard repairs are allowed before soft repair	Any outstanding soft repairs must be cleared before a hard repair	Clearing occurs by either: (a) powerdown and power-up sequence or (b) Reset and re-initialize.
Repair Sequence	1 method – WR cmd.	2 methods WRA and WR	

Entry into sPPR is through a register enable, ACT command is used to transmit the bank and row address of the row to be replaced in DRAM. After tRCD time, a WR command is used to select the individual DRAM through the DQ bits and to transfer the repair address into an internal register in the DRAM. After a write recovery time and PRE, the sPPR mode can be exited and normal operation can resume. Care must be taken that refresh is not violated for the other rows in the array during soft repair time. Also note that the DRAM will retain the soft repair information inside the DRAM as long as VDD remains within the operating region. If DRAM power is removed or the DRAM is RESET, the soft repair will revert to the un-repaired state. PPR and sPPR may not be enabled at the same time. sPPR must have been disabled and cleared prior to entering PPR mode.

With sPPR, DDR4 can repair one Row per Bank Group. When the hard PPR resources for a bank group are used up, the bank group has no more available resources for soft PPR. If a repair sequence is issued to a bank group with no repair resource available,

the DRAM will ignore the programming sequence. sPPR mode is optional for 4Gb & 8Gb density DDR4 devices and required for greater than 8Gb densities.

2.33.1 Soft Repair of a Fail Row Address

The following is the procedure of sPPR with WR command. Note that during the soft repair sequence, no refresh is allowed.

1. Before entering ‘sPPR’ mode, all banks must be Precharged; DBI and CRC Modes must be disabled
2. Enable sPPR using MR4 bit “A5=1” and wait tMOD
3. Issue ACT command with the Bank and Row Fail address, Write data is used to select the individual DRAM in the Rank for repair.
4. A WR command is issued after tRCD, with VALID column address. The DRAM will ignore the column address given with the WR command.
5. After WL (WL=CWL+AL+PL), all of the DQs of the individual Target DRAM should be LOW for 4tCK. If any DQ is high during 4tCK burst, then the sPPR protocol will not be executed. If more than one DRAM shares the same command bus, DRAMs that are not being repaired should have all of their DQ’s driven HIGH for 4tCK. If all of the DQ’s are neither all LOW nor all HIGH for 4tCK, then sPPR mode will not be executed.
6. Wait tWR for the internal repair register to be written and then issue PRE to the Bank.
7. Wait 20ns after PRE which allow DRAM to recognize repaired Row address
8. Exit PPR with setting MR4 bit “A5=0” and wait tMOD
9. Only one soft repair per Bank Group is allowed before a hard repair is required. In the case of a failing address in a different Bank Group, Repeat Step 2 to 8. During a soft Repair, Refresh command is not allowed between sPPR MRS entry and exit.
   Once sPPR mode is exited, to confirm if target row is repaired correctly, the host can verify the repair by writing data into the target row and reading it back after PPR exit with MR4 [A5=0].

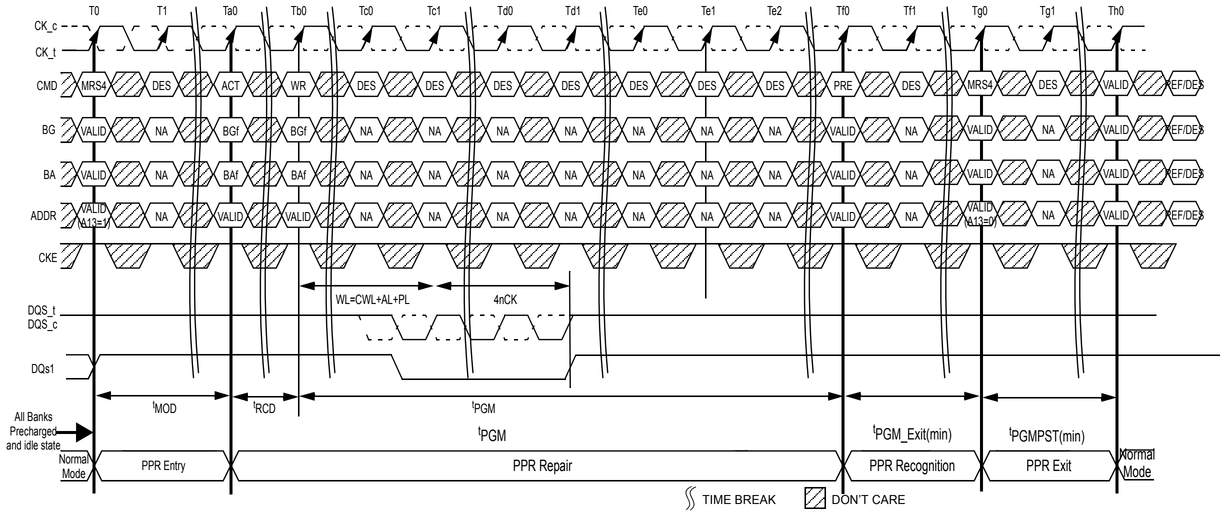


Figure 168. Fail Row Soft PPR (WR Case)

2.34 TRR Mode - Target Row Refresh

A DDR4 SDRAM's row has a limited number of times a given row can be accessed within a certain time period prior to requiring adjacent rows to be refreshed. The Maximum Activate Count (MAC) is the maximum number of activates that a single row can sustain within a time interval of equal to or less than the Maximum Activate Window (tMAW) before the adjacent rows need to be refreshed regardless of how the activates are distributed over tMAW. The row receiving the excessive actives is the Target Row (TRn), the two adjacent rows to be refreshed are the victim rows.

When the MAC limit is reached on TRn, either the SDRAM must receive roundup(tMAW / tREFI) Refresh Commands (REF) before another row activate is issued, or the DDR4 SDRAM should be placed into Targeted Row Refresh (TRR) mode. The TRR Mode will refresh the rows adjacent to the TRn that encountered MAC limit. There could be one or two target rows in a bank associated to one victim row. The cumulative value of the Activates from two target rows on a victim row should not exceed MAC value as well.

When the Temperature Controlled Refresh (TCR) mode is enabled (MR4 A3='1'), tMAW should be adjusted depending on the TCR range (MR4 A2) as shown in the Table 72.

[Table 80] tMAW adjustment when Temperature Controlled Refresh (TCR) mode is enabled

MR4 A3 (TCR mode)	MR4 A2 (TCR range)	tMAW	Note
0 (disabled)	don't care	tMAW(base)	1
1 (enabled)	0 (normal range)	≤ 4*tMAW(base)	1
	1 (extended range)	≤ 8*tMAW(base)	1

NOTE
1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to get the value for tMAW(base). tMAW(base) cannot be greater than 8192*tREFI(base).

Table 73 shows MR2 fields required to support the new TRR settings. Setting MR2 [A13=1] enables TRR Mode and setting MR2 [A13=0] disables TRR Mode. MR2 [A8, A2] defines the bank group (BGn) to which TRR will be applied to and MR2 [A1, A0] defines which bank (BAn) the target row is located in.

The TRR mode must be disabled during initialization as well as any other DDR4 SDRAM calibration modes. The TRR mode is entered from a DRAM Idle State, once TRR mode has been entered, no other Mode Register commands are allowed until TRR mode is completed, except setting MR2 [A13=0] to interrupt and reissue the TRR mode is allowed in the case such as the DRAM receiving a Parity error during TRR mode.

When enabled; TRR Mode is self-clearing; the mode will be disabled automatically after the completion of defined TRR flow; after the 3rd BGn precharge has completed plus tMOD. Optionally the TRR mode can also be exited via another MRS command at the completion of TRR by setting MR2 [A13=0]; if the TRR is exited via another MRS command, the value written to MR2 [A8, A2:A0] are don't cares.

2.34.1 TRR Mode Operation

1. The timing diagram in Figure 170 depicts TRR mode. The following steps must be performed when TRR mode is enabled. This mode requires all three ACT (ACT1, ACT2 and ACT3) and three corresponding PRE commands (PRE1, PRE2 and PRE3) to complete TRR mode. A Precharge All (PREA) commands issued while DDR4 SDRAM is in TRR mode will also perform precharge to BGn and counts towards a PREn command.

2. Prior to issuing the MRS command to enter TRR mode, the SDRAM should be in the idle state. A MRS command must be issued with MR2 [A13=1], MR2[A8,A2] containing the targeted bank group and MR2 [A1,A0] defining the bank in which the targeted row is located. All other MR2 bits should remain unchanged.

3. No activity is to occur in the DRAM until tMOD has been satisfied. Once tMOD has been satisfied, the only commands to BGn allowed are ACT and PRE until the TRR mode has been completed.

4. The first ACT to the BGn with the TRn address can now be applied, no other command is allowed at this point. All other bank groups must remain inactive from when the first BGn ACT command is issued until [(1.5 * tRAS) + tRP] is satisfied.

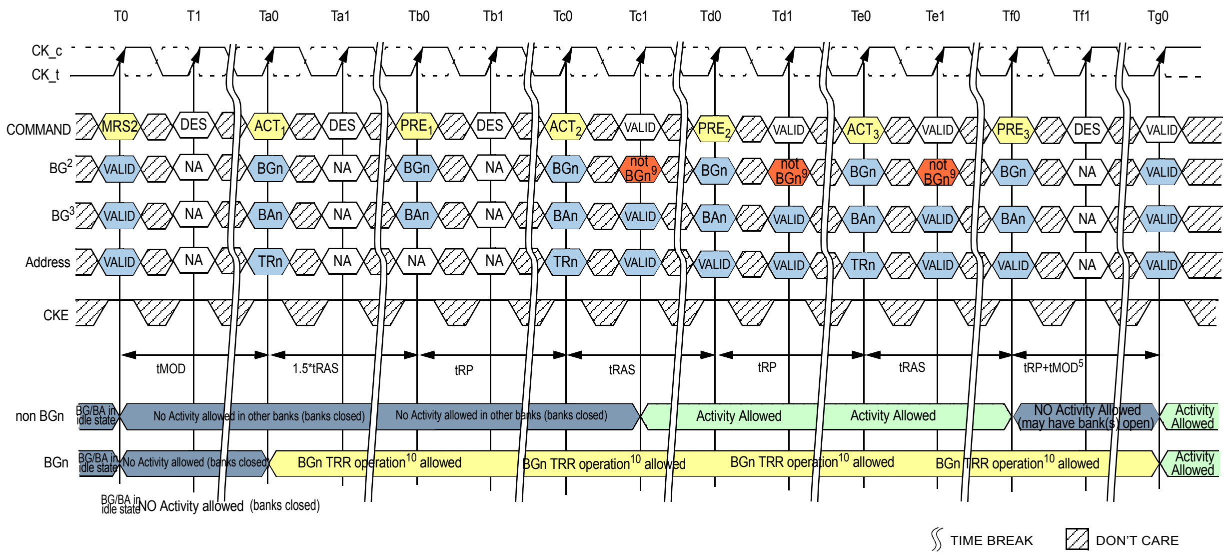
5. After the first ACT to the BGn with the TRn address is issued, a PRE to BGn is to be issued (1.5 * tRAS) later; and then followed tRP later by the second ACT to the BGn with the TRn address. Once the 2nd activate to the BGn is issued, nonBGn bank groups are allowed to have activity.

6. After the second ACT to the BGn with the TRn address is issued, a PRE to BGn is to be issued tRAS later and then followed tRP later by the third ACT to the BGn with the TRn address.

7. After the third ACT to the BGn with the TRn address is issued, a PRE to BGn would be issued tRAS later; and once the third PRE has been issued, nonBGn bank groups are not allowed to have activity until TRR mode is exited. The TRR mode is completed once tRP plus tMOD is satisfied.

8. TRR mode must be completed as specified to guarantee that adjacent rows are refreshed. Anytime the TRR mode is interrupted and not completed, such as the DRAM receiving a Parity error during TRR mode, the interrupted TRR Mode must be cleared and then subsequently performed again. To clear an interrupted TRR mode, an MR2 change is required with setting MR2 [A13=0],
MR2 [A8,A2:A0] are don't care, followed by three PRE to BGn, tRP time in between each PRE command. When a Parity error occurs in TRR Mode, the SDRAM may self-clear MR2 [A13=0]. The complete TRR sequence (Steps 2-7) must be then re-issued and completed to guarantee that the adjacent rows are refreshed.

9. Refresh command to the DDR4 SDRAM or entering Self-Refresh mode is not allowed while the DRAM is in TRR mode.



NOTE:
1. TRn is targeted row.
2. Bank group BGn represents the bank group which the targeted row is located.
3. Bank Address BAn represents the bank which the targeted row is located.
4. TRR mode self-clears after tMOD+tRP measured from 3rd BGn precharge PRE_3 at clock edge Tg0.
5. TRR mode or any other activity can be re-engaged after tMOD+tRP from 3rd BGn precharge PRE_3. PRE_ALL also counts if issued instead of PREn. TRR mode is cleared by DRAM after PRE_3 to the BGn bank.

6. Activate commands to BGn during TRR Mode do not provide refreshing support, i,e. the Refresh counter is unaffected.
7. The DRAM must restore the degraded row(s) caused by excessive activation of the targeted row(TRn) neccessary to meet refresh requirements.
8. A new TRR mode must wait tMOD+tRP time after the third precharge.
9. BGn may not be used with any other command.
10. ACT and PRE are the only allowed commands to BGn during TRR mode.
11. Refresh commands are not allowed during TRR mode.
12. All DRAM timings are to be met by DRAM during TRR mode such as tFAW. Issuing of ACT1,ACT2 and ACT3 counts towards tFAW budget.

Figure 169. TRR Mode

2.34.2 MR2 Register Definition

The mode register controls for TRR Mode are shown in Table 69.

[Table 81] MR2 Register Definition for TRR Mode

Address	Operating Mode	Description
A13	TRR Mode	0 = Disabled 1 = Enabled
A8, A2	TRR Mode - BGn	00 = BG0 10 = BG2 01 = BG1 11 = BG3
A1, A0	TRR Mode - BAn	00 = Bank 0 10 = Bank 2 01 = Bank 1 11 = Bank 3

2.35 3DS SDRAM Command Description and Operation

2.35.1 ACTIVATE Command

In a 3D Stacked DDR4 SDRAM the single chip select pin and the C[2:0] pins select the logical rank.

The value on the BA0 - BA1 and BG0 - BG1 inputs selects the bank, the chip ID inputs select the logical ranks and the address provided on inputs A0-A17 selects the row. This row remains open (or active) for accesses until a precharge command is issued to that bank in that logical rank. A PRECHARGE command must be issued (to that bank in that logical rank) before opening a different row in the same bank in the same logical rank.

The minimum time interval between successive ACTIVATE commands to the same bank of a DDR SDRAM is defined by tRC. The minimum time interval between successive ACTIVATE commands to different banks within the same bank group of a DDR4 SDRAM is defined by tRRD_L (Min). The minimum time interval between successive ACTIVATE commands to different banks within different bank groups of a DDR4 SDRAM is defined by tRRD_S (Min). For a DDR4 3DS device, the timing parameters that applies to successive ACTIVATE commands to different banks in the same logical rank are defined as tRRD_S_slr (Min) and tRRD_L_slr (Min). The timing parameter that applies to successive ACTIVATE commands to different logical ranks is defined as tRRD_dlr (Min).

No more than four bank ACTIVATE commands may be issued in a given tFAW_slr (Min) period to the same logical rank. For all logical ranks in a 3DS device, the tFAW_dlr timing constraint applies, i.e. no more than four bank ACTIVATE commands to the whole 3DS SDRAM may be issued in a given tFAW_dlr (Min) period.

The timing restrictions covering ACTIVATE commands are documented in Table 82.

[Table 82] Truth Table for ACTIVATE Command

Symbol	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7
ACTIVATE (ACT)	L	L	L	L	ACT	DES	DES	DES	DES	DES	DES	DES
ACTIVATE (ACT)	L	L	L	H	DES	ACT	DES	DES	DES	DES	DES	DES
ACTIVATE (ACT)	L	L	H	L	DES	DES	ACT	DES	DES	DES	DES	DES
ACTIVATE (ACT)	L	L	H	H	DES	DES	DES	ACT	DES	DES	DES	DES
ACTIVATE (ACT)	L	H	L	L	DES	DES	DES	DES	ACT	DES	DES	DES
ACTIVATE (ACT)	L	H	L	H	DES	DES	DES	DES	DES	ACT	DES	DES
ACTIVATE (ACT)	L	H	H	L	DES	DES	DES	DES	DES	DES	ACT	DES
ACTIVATE (ACT)	L	H	H	H	DES	DES	DES	DES	DES	DES	DES	ACT
Any command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES

NOTE:
1. "V" means H or L (but a defined logic level).

2.35.2 Precharge and Precharge All Commands

The Single Bank Precharge (PRE) and Precharge All Banks (PREA) commands apply only to a single logical rank of a 3D Stacked SDRAM. PRE commands (or PRE commands to each open bank) have to be issued to all logical ranks with open banks before the device can enter Self Refresh mode.

DDR4 3D Stacked SDRAMs have the same values for tRP, tRTP, tRAS and tDAL as planar DDR4 SDRAMs of the same frequency.

Table 83 and Table 84 show the truth tables for Precharge and Precharge All commands.

[Table 83] Truth Table for Precharge

Symbol	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	NOTE
Precharge (PRE)	L	L	L	L	PRE	DES	DES	DES	DES	DES	DES	DES	1,3
Precharge (PRE)	L	L	L	H	DES	PRE	DES	DES	DES	DES	DES	DES	1,3
Precharge (PRE)	L	L	H	L	DES	DES	PRE	DES	DES	DES	DES	DES	1,3
Precharge (PRE)	L	L	H	H	DES	DES	DES	PRE	DES	DES	DES	DES	1,3
Precharge (PRE)	L	H	L	L	DES	DES	DES	DES	PRE	DES	DES	DES	1,3
Precharge (PRE)	L	H	L	H	DES	DES	DES	DES	DES	PRE	DES	DES	1,3
Precharge (PRE)	L	H	H	L	DES	DES	DES	DES	DES	DES	PRE	DES	1,3
Precharge (PRE)	L	H	H	H	DES	DES	DES	DES	DES	DES	DES	PRE	1,3
Any command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	2

NOTE:
1. Precharge only to the same selected bank within selected logical rank(s)
2. "V" means H or L (but a defined logic level)
3. A10=L

[Table 84] Truth Table for Precharge All

Symbol	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	NOTE
Precharge All (PREA)	L	L	L	L	PREA	DES	DES	DES	DES	DES	DES	DES	1,3
Precharge All (PREA)	L	L	L	H	DES	PREA	DES	DES	DES	DES	DES	DES	1,3
Precharge All (PREA)	L	L	H	L	DES	DES	PREA	DES	DES	DES	DES	DES	1,3
Precharge All (PREA)	L	L	H	H	DES	DES	DES	PREA	DES	DES	DES	DES	1,3
Precharge All (PREA)	L	H	L	L	DES	DES	DES	DES	PREA	DES	DES	DES	1,3
Precharge All (PREA)	L	H	L	H	DES	DES	DES	DES	DES	PREA	DES	DES	1,3
Precharge All (PREA)	L	H	H	L	DES	DES	DES	DES	DES	DES	PREA	DES	1,3
Precharge All (PREA)	L	H	H	H	DES	DES	DES	DES	DES	DES	DES	PREA	1,3
Any command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	2

NOTE:
1. Precharge only to the same selected bank within selected logical rank(s)
2. "V" means H or L (but a defined logic level)
3. A10=L

2.35.3 Read and Write Commands

In a DDR4 3D Stacked SDRAM the single select pin and the C[2:0] pins select the logical rank.

The DDR4 3DS command to command timings are shown in Table 85 and Table 86.

[Table 85] Minimum Read and Write Command Timings for 2H and 4H devices

<table>
<tr><th>Logical Rank</th><th>Bank Group</th><th>Timing Parameter</th><th>DDR4-1600</th><th>DDR4-1866</th><th>DDR4-2133</th><th>Units</th><th>Note</th></tr>
<tr><td rowspan="8">Same</td><td rowspan="4">Same</td><td>Minimum Read to Read</td><td rowspan="2">5</td><td rowspan="2">5</td><td rowspan="2">6</td><td rowspan="2">nCK</td><td rowspan="2">1</td></tr>
<tr><td>Minimum Write to Write</td></tr>
<tr><td>Minimum Read to Write</td><td colspan="4">CL - CWL + RBL / 2 + 1 tCK + tWPRE</td><td>1,2</td></tr>
<tr><td>Minimum Read after Write</td><td colspan="4">CWL + WBL / 2 + tWTR_L</td><td>1,3</td></tr>
<tr><td rowspan="4">different</td><td>Minimum Read to Read</td><td rowspan="2">4</td><td rowspan="2">4</td><td rowspan="2">4</td><td rowspan="2">nCK</td><td rowspan="2">1</td></tr>
<tr><td>Minimum Write to Write</td></tr>
<tr><td>Minimum Read to Write</td><td colspan="4">CL - CWL + RBL / 2 + 1 tCK + tWPRE</td><td>1,2</td></tr>
<tr><td>Minimum Read after Write</td><td colspan="4">CWL + WBL / 2 + tWTR_S</td><td>1,3</td></tr>
<tr><td rowspan="8">different</td><td rowspan="4">Same</td><td>Minimum Read to Read</td><td rowspan="2">4</td><td rowspan="2">4</td><td rowspan="2">5(4)
(optional)</td><td rowspan="2">nCK</td><td rowspan="2">1</td></tr>
<tr><td>Minimum Write to Write</td></tr>
<tr><td>Minimum Read to Write</td><td colspan="4">CL - CWL + RBL / 2 + 1 tCK + tWPRE</td><td>1,2</td></tr>
<tr><td>Minimum Read after Write</td><td colspan="4">CWL + WBL / 2 + tWTR_S</td><td>1,3</td></tr>
<tr><td rowspan="4">different</td><td>Minimum Read to Read</td><td rowspan="2">4</td><td rowspan="2">4</td><td rowspan="2">5(4)
(optional)</td><td rowspan="2">nCK</td><td rowspan="2">1</td></tr>
<tr><td>Minimum Write to Write</td></tr>
<tr><td>Minimum Read to Write</td><td colspan="4">CL - CWL + RBL / 2 + 1 tCK + tWPRE</td><td>1,2</td></tr>
<tr><td>Minimum Read after Write</td><td colspan="4">CWL + WBL / 2 + tWTR_S</td><td>1,3</td></tr>
</table>

Note:
1. These timings require extended calibrations times tZQinit and tZQCS (values TBD).
2. RBL : Read burst length associated with Read command
   RBL = 8 for fixed 8 and on-the-fly mode 8
   RBL = 4 for fixed BC4 and on-the-fly mode BC4
3. WBL : Write burst length associated with Write command
   WBL = 8 for fixed 8 and on-the-fly mode 8 or BC4
   WBL = 4 for fixed BC4 only

[Table 86] Minimum Read and Write Command Timings for 8H devices

<table>
<tr><th>Logical Rank</th><th>Bank Group</th><th>Timing Parameter</th><th>DDR4-1600</th><th>DDR4-1866</th><th>DDR4-2133</th><th>Units</th><th>Note</th></tr>
<tr><td rowspan="8">Same</td><td rowspan="4">Same</td><td>Minimum Read to Read</td><td rowspan="2">TBD</td><td rowspan="2">TBD</td><td rowspan="2">TBD</td><td rowspan="2">nCK</td><td rowspan="2">1</td></tr>
<tr><td>Minimum Write to Write</td></tr>
<tr><td>Minimum Read to Write</td><td colspan="4">TBD</td><td>1,2</td></tr>
<tr><td>Minimum Read after Write</td><td colspan="4">TBD</td><td>1,3</td></tr>
<tr><td rowspan="4">different</td><td>Minimum Read to Read</td><td rowspan="2">TBD</td><td rowspan="2">TBD</td><td rowspan="2">TBD</td><td rowspan="2">nCK</td><td rowspan="2">1</td></tr>
<tr><td>Minimum Write to Write</td></tr>
<tr><td>Minimum Read to Write</td><td colspan="4">TBD</td><td>1,2</td></tr>
<tr><td>Minimum Read after Write</td><td colspan="4">TBD</td><td>1,3</td></tr>
<tr><td rowspan="8">different</td><td rowspan="4">Same</td><td>Minimum Read to Read</td><td rowspan="2">TBD</td><td rowspan="2">TBD</td><td rowspan="2">TBD</td><td rowspan="2">nCK</td><td rowspan="2">1</td></tr>
<tr><td>Minimum Write to Write</td></tr>
<tr><td>Minimum Read to Write</td><td colspan="4">TBD</td><td>1,2</td></tr>
<tr><td>Minimum Read after Write</td><td colspan="4">TBD</td><td>1,3</td></tr>
<tr><td rowspan="4">different</td><td>Minimum Read to Read</td><td rowspan="2">TBD</td><td rowspan="2">TBD</td><td rowspan="2">TBD</td><td rowspan="2">nCK</td><td rowspan="2">1</td></tr>
<tr><td>Minimum Write to Write</td></tr>
<tr><td>Minimum Read to Write</td><td colspan="4">TBD</td><td>1,2</td></tr>
<tr><td>Minimum Read after Write</td><td colspan="4">TBD</td><td>1,3</td></tr>
</table>

NOTE:
1. These timings require extended calibrations times tZQinit and tZQCS (values TBD).

2.35.4 Refresh Command

No more than one logical rank Refresh Command can be initiated simultaneously to DDR4 3D Stacked SDRAMs as shown in Table.

The minimum refresh cycle time to a single logical rank (=tRFC_slr) has the same value as tRFC for a planar DDR4 SDRAM of the same density as the logical rank.

The minimum time between issuing refresh commands to different logical ranks is specified as tRFC_dlr. After a Refresh command to a logical rank, other valid commands can be issued before tRFC_dlr to the other logical ranks that are not the target of the refresh.

[Table 87] Truth Table for Refresh Command

Symbol	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	NOTE
Refresh (REF)	L	L	L	L	**REF**	DES	DES	DES	DES	DES	DES	DES	1
Refresh (REF)	L	L	L	H	DES	**REF**	DES	DES	DES	DES	DES	DES	1
Refresh (REF)	L	L	H	L	DES	DES	**REF**	DES	DES	DES	DES	DES	1
Refresh (REF)	L	L	H	H	DES	DES	DES	**REF**	DES	DES	DES	DES	1
Refresh (REF)	L	H	L	L	DES	DES	DES	DES	**REF**	DES	DES	DES	1
Refresh (REF)	L	H	L	H	DES	DES	DES	DES	DES	**REF**	DES	DES	1
Refresh (REF)	L	H	H	L	DES	DES	DES	DES	DES	DES	**REF**	DES	1
Refresh (REF)	L	H	H	H	DES	DES	DES	DES	DES	DES	DES	**REF**	1
Any command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	1,2

NOTE:
1. CKE=H
2. "V" means H or L (but a defined logic level)

In general, a Refresh command needs to be issued to each logical rank in 3D Stacked DDR4 SDRAM regularly every tREFI_slr interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands per logical rank can be postponed during operation of the 3D stacked DDR4 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed per logical rank. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI_slr. A maximum of 8 additional Refresh commands can be issued in advance ("pulled in") per logical rank, with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI_slr. At any given time, a maximum of 16 REF commands per logical rank can be issued within 2 x tREFI_slr. Self-Refresh Mode may be entered with a maximum of eight Refresh commands per logical rank being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight per logical rank. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

2.35.5 Self-Refresh Operation and Power-Down Modes

The CKE functionality should adhere to the DDR4 specification for planar DDR4 SDRAMs. Since there is only one CKE pin per 3DS device, all logical ranks enter self refresh and power down together, as shown in Table 88.

[Table 88] Truth Table for Refresh Command

Symbol	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	NOTE
Refresh (REF)	L	V	V	V	SRE	SRE	SRE	SRE	SRE	SRE	SRE	SRE	1,2
Refresh (REF)	H	V	V	V	PDE	PDE	PDE	PDE	PDE	PDE	PDE	PDE	1,2
Refresh (REF)	L	V	V	V	PDE	PDE	PDE	PDE	PDE	PDE	PDE	PDE	1,2
Any command	H	V	V	V	PDE	PDE	PDE	PDE	PDE	PDE	PDE	PDE	1,2

NOTE:
1. "V" means H or L (but a defined logic level)
2. with CKE H-->L

Self-Refresh exit (SRX) and power-down exit (PDX) apply to all logical ranks in a 3D Stacked device and is caused by the Low-to-High transition of the single CKE pin.

A Deselect command must be used for SRX.

A Deselect command must be used for PDX.

3D Stacked SDRAMs have the same values of all parameters for Self Refresh Timings and Power DownTimings as planar DDR4 SDRAMs of the same frequency. Specification of tXS DDR4 3DS has been modified with Refresh Parameter by Logical Rank Density.

Once a Self-Refresh Exit command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress.The use of Self- Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR4 3D stacked SDRAM requires a minimum of one extra refresh command to all logical Ranks (each refresh period of tRFC_slr), before it is put back into Self-Refresh Mode.

2.35.6 Write Leveling

The memory controller initiates Leveling mode of all SDRAMs by setting bit A7 of MR1 to 1. Upon entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only DESELECT commands are allowed, as well as an MRS command to exit write leveling mode. Since the controller levels one rank at a time, the output of other physical ranks must be disabled by setting MR1 bit A12 to 1.

2.35.7 ZQ Calibration Commands

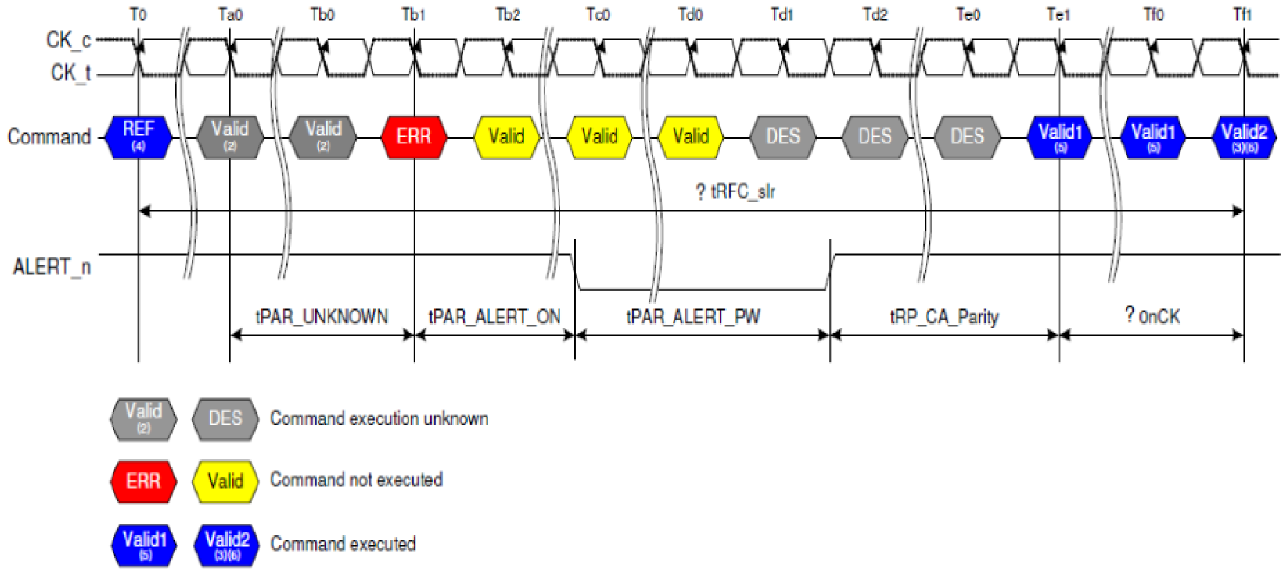
Each 3DS package will have a single ZQ calibration pin, independent of the number of logical ranks in the stack. Since there is only one I/O per device, the ZQ pin should be associated with the master die.

The calibration procedure and the result should adhere to JEDEC DDR4 component specification
(JESD79-XX). The host may issue ZQ calibration command to each logical rank. The SDRAM can choose to ignore the ZQ commands to the non-master logical rank or execute the calibration of the I/O attached to the master die.

2.35.8 Command Address Parity (CA Parity)

C/A Parity signal (PAR) covers ACT_n, RAS_n, CAS_n, WE_n and the address bus including bank address, bank group bits and chip ID bits C[2:0]. The control signals CKE, ODT and CS_n are not included. (e.g. for a 4 Gbit x4 monolithic device, parity is computed across BG0, BG1, BA1, BA0, A16/ RAS_n, A15/CAS_n, A14/WE_n, A13-A0 and ACT_n). (DRAM should internally treat any unused address pins as 0's, e.g. if a common die has stacked pins C[2:0] but the device is used in a monolithic or less than 8H stacked application then the unused address pins should internally be treated as 0's).

When Refresh commands are issued to logical ranks prior to a Error command on the other rank, 3DS DDR4 shall finish the on-going Refresh operation. Upon Alert Pulse Width deactivation, DRAM conducts Precharge-All operation to the logical ranks which are not on Refresh operation to make them ready for valid commands. After tRP_CA_Parity from the end of tPAR_ALERT_PW, valid commands can be issued to the logical ranks which do not have on-going Refresh operation. Valid commands, including MRS, to the logical ranks with on-going Refresh can be issued after both tRFC_slr and tRP_CA_Parity are met as illustrated in Figure 170.



NOTE:
1. DRAM is emptying queues, Precharge All and parity cheching off until Parity Error Status bit cleared.
2. Command execution is unkown the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
3. Normal operation with parity latency (CA Parity Persistent Error Mode Disabled). Parity checking off until Parity Error Status bit cleared.
4. When REF is issued in tPAR_UNKNOWN range, REF may not be executed. But, host must wait tRFC_slr to issue valid commands to the same logical rank.
5. Valid commands to the rank with no on-going REFare available.
6. Valid commands, including MRS, to the rank with on-going REF are available.

Figure 170. DDR4 3DS SDRAM Refresh Operation

[Table 89] The timing delay for Valid commands from Alert Pulse deassertion

Parameter	Symbol	DDR4-1600/1866/2133	Units	Note
Minimum time for valid commnads except for MRS to the logical ranks that do not conduct REF	tRP_CA_Parity	TBD	nCK	

2.35.9 Target Row Refresh (TRR)

For DRAM to operate TRR function independantly on the selected logical rank, logical rank information (C0, C1 and C2) should be given to DRAM at the TRR mode entry (MR2 A13=H) and disable (MR2 A13=L) along with Bank and Bank Group Address.

2.35.10 Post Package Repair (PPR)

For DRAM to operate PPR function independantly on the selected logical rank, logical rank information(C0, C1 and C2) should be given to DRAM at the ACT, WR, WRA, REF and PRE during PPR mode.

In case of PPR with WRA, REF (1x) commands are allowed from PL+WL+BL/2+tWR+tRP after WRA command during tPGM and tPGMPST for proper repair. Upon receiving REF (1x) command, DRAM performs normal Refresh operation and maintains the array content except for the Bank containing row that is being repaired. Other commands except REF during tPGM can cause incomplete repair so no other command except REF to the banks and logical ranks which do not have on-going PPR is allowed during tPGM.

3. On-Die Termination

ODT (On-Die Termination) is a feature of the DDR4 SDRAM that allows the DRAM to change termination resistance for each DQ, DQS_t, DQS_c and DM_n for x4 and x8 configuration (and TDQS_t, TDQS_c for X8 configuration, when enabled via A11=1 in MR1) via the ODT control pin or Write Command or Default Parking value with MR setting. For x16 configuration, ODT is applied to each DQU, DQL, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n and DML_n signal. The ODT feature is designed to improve signal integ-rity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document :

- The ODT control modes are described in Section 3.1.
- The ODT synchronous mode is described in Section 3.2
- The Dynamic ODT feature is described in Section 3.3
- The ODT asynchronous mode is described in Section 3.4
- The ODT buffer disable mode is described in “ODT buffer disabled mode for Power down” in Section 3.5

The ODT feature is turned off and not supported in Self-Refresh mode. A simple functional representation of the DRAM ODT feature is shown in Figure 170.

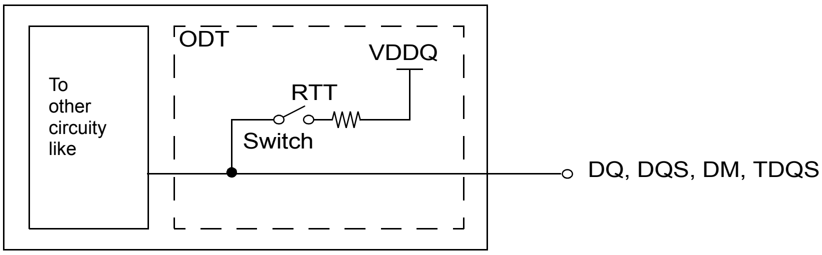


Figure 171. Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and Mode Register Setting and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see Section 1.5). The ODT pin will be ignored if the Mode Registers MR1 is programmed to disable RTT_NOM(MR1{A10,A9,A8}={0,0,0}) and in self-refresh mode.

3.1 ODT Mode Register and ODT State Table

The ODT Mode of DDR4 SDRAM has 4 states, Data Termination Disable, RTT_WR, RTT_NOM and RTT_PARK. And the ODT Mode is enabled if any of MR1{A10,A9,A8} or MR2 {A10:A9} or MR5 {A8:A6} are non zero. In this case, the value of RTT is determined by the settings of those bits.
After entering Self-Refresh mode, DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of these setting.

Application: Controller can control each RTT condition with WR/RD command and ODT pin

- RTT_WR: The rank that is being written to provide termination regardless of ODT pin status (either HIGH or LOW)
- RTT_NOM: DRAM turns ON RTT_NOM if it sees ODT asserted (except ODT is disabled by MR1).
- RTT_PARK: Default parked value set via MR5 to be enabled and ODT pin is driven LOW.
- Data Termination Disable: DRAM driving data upon receiving READ command disables the termination after RL-X and stays off for a duration of BL/2 + X + Y clock cycles.

X is 2 for 1tCK and 3 for 2tCK preamble mode.
Y is 0 when CRC is disabled and 1 when it's enabled
- The Termination State Table is shown in Table 75.

Those RTT values have priority as following.
1. Data Termination Disable
2. RTT_WR
3. RTT_NOM
4. RTT_PARK

which means if there is WRITE command along with ODT pin HIGH, then DRAM turns on RTT_WR not RTT_NOM, and also if there is READ command, then DRAM disables data termination regardless of ODT pin and goes into Driving mode.

[Table 90] Termination State Table

RTT_PARK MR5{A8:A6}	RTT_NOM MR1 {A10:A9:A8}	ODT pin	DRAM termination state	Note
Enabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	RTT_PARK	1,2
	Disabled	Don't care[3]	RTT_PARK	1,2
Disabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	Hi-Z	1,2
	Disabled	Don't care[3]	Hi-Z	1,2

NOTE :
1. When read command is executed, DRAM termination state will be Hi-Z for defined period independent of ODT pin and MR setting of RTT_PARK/RTT_NOM.
2. If RTT_WR is enabled, RTT_WR will be activated by Write command for defined period time independent of ODT pin and MR setting of RTT_PARK /RTT_NOM.
3. If RTT_NOM MRS is disabled, ODT receiver power will be turned off to save power.

On-Die Termination effective resistance RTT is defined by MRS bits.
ODT is applied to the DQ, DM, DQS_T/DQS_C and TDQS_T/TDQS_C (x8 devices only) pins.
A functional representation of the on-die termination is shown in the figure below.

$$RTT = \frac{VDDQ - Vout}{|\ I\ out\ |}$$

Chip In Termination Mode

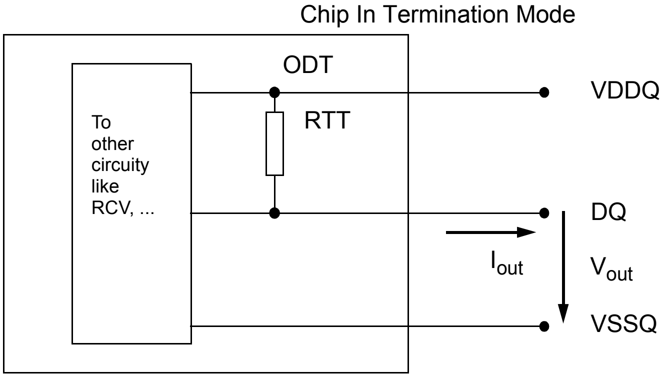


Figure 172. On Die Termination

On die termination effective Rtt values supported are 240, 120, 80, 60, 48, 40, 34 ohms.

[Table 91] ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration

ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration

RTT	Vout	Min	Nom	Max	Unit	NOTE
240Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
120Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/2	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/2	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/2	1,2,3
80Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/3	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/3	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/3	1,2,3
60Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/4	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/4	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/4	1,2,3
48Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2,3
40Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/6	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/6	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/6	1,2,3
34Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2,3
DQ-DQ Mis-match within byte	VOMdc = 0.8* VDDQ	0	-	0	%	1,2,4,5,6

NOTE :

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 1.1*VDDQ.
3. 3. The tolerance limits are specified under the condition that VDDQ=VDD and VSSQ=VSS
4. DQ to DQ mismatch within byte variation for a given component including DQS_T and DQS_C (characterized)
5. RTT variance range ratio to RTT Nominal value in a given component, including DQS_t and DQS_c.

$$\text{DQ-DQ Mismatch in a Device} = \frac{\text{RTTMax} - \text{RTTMin}}{\text{RTTNOM}} * 100$$

6. This parameter of x16 device is specified for Upper byte and Lower byte.

3.2 Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode
- Precharge power down mode

In synchronous ODT mode, RTT_NOM will be turned on DODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turned off DODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The ODT latency is tied to the Write Latency (WL = CWL + AL + PL) by: DODTLon = WL - 2; DODTLoff = WL - 2.
When operating in 2tCK Preamble Mode, The ODT latency must be 1 clock smaller than in 1tCK Preamble Mode; DODTLon =WL - 3; DODTLoff = WL - 3."(WL = CWL+AL+PL)

3.2.1 ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) and the Parity Latency (PL) programmed into the Mode Register (MR1) applies to ODT Latencies as shown inTable 77 and Table 78. For details, refer to DDR4 SDRAM latency definitions.

[Table 92] ODT Latency

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200	Unit
DODTLon	Direct ODT turn on Latency	CWL + AL + PL - 2.0	tCK
DODTLoff	Direct ODT turn off Latency	CWL + AL + PL - 2.0	
RODTLoff	Read command to internal ODT turn off Latency	See detail Table 78	
RODTLon4	Read command to RTT_PARK turn on Latency in BC4	See detail Table 78	
RODTLon8	Read command to RTT_PARK turn on Latency in BC8/BL8	See detail Table 78	

[Table 93] Read command to ODT off/on Latency variation by Preamble and CRC

Symbol	1tck Preamble	2tck Preamble	Unit
	CRC off	CRC off	
RODTLoff	CL+AL+PL-2.0	CL+AL+PL-3.0	tCK
RODTLon4	RODTLoff +4	RODTLoff +5	
RODTLon8	RODTLoff +6	RODTLoff +7	
ODTH4	4	5	
ODTH8	6	7	

3.2.2 Timing Parameters

In synchronous ODT mode, the following timing parameters apply:

DODTLon, DODTLoff, RODTLoff, RODTLon4, RODTLon8, tADC,min,max.

tADC,min and tADC,max are minimum and maximum RTT change timing skew between different termination values. Those timing parameters apply to both the Synchronous ODT mode and the Data Termination Disable mode.

When ODT is asserted, it must remain HIGH until minimum ODTH4 (BL=4) or ODTH8 (BL=8) is satisfied. Additionally, depending on CRC or 2tCK preamble setting in MRS, ODTH should be adjusted.

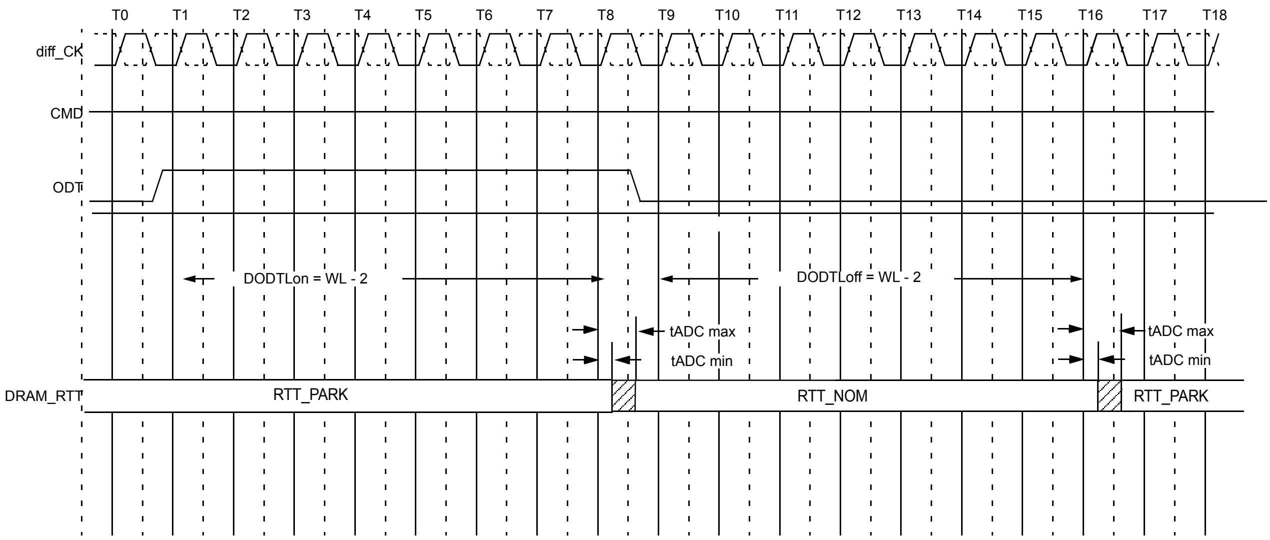


Figure 173. Synchronous ODT Timing Example for CWL=9, AL=0, PL=0; DODTLon=WL-2=7; DODTLoff=WL-2=7

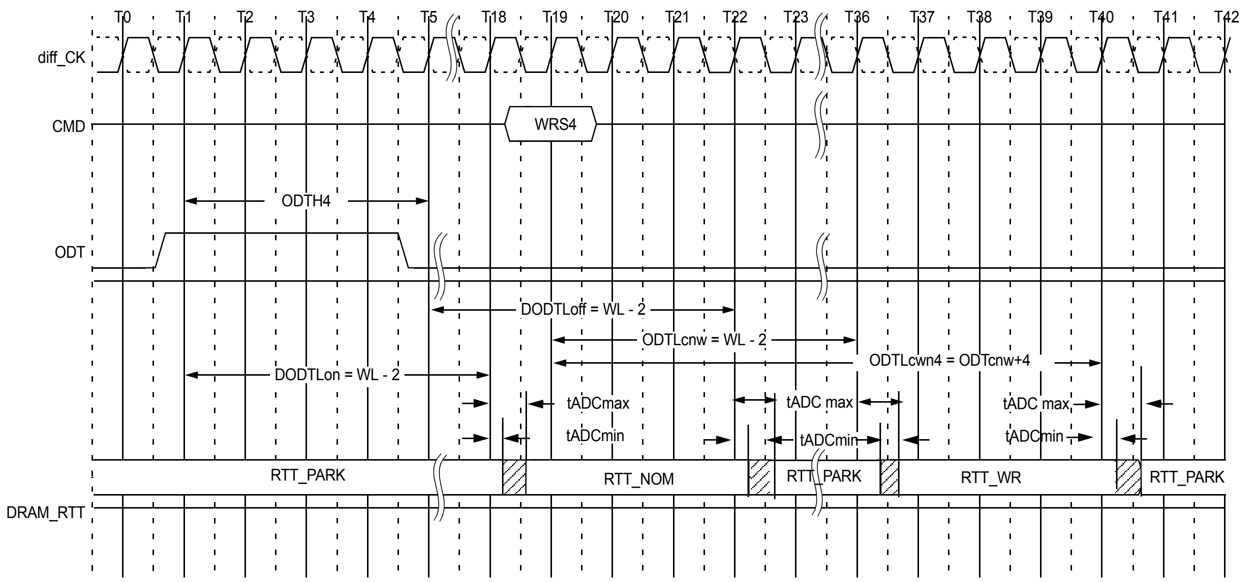


Figure 174. Synchronous ODT example with BL=4, CWL=9, AL=10, PL=0; DODTLon/off=WL-2=17, ODTcnw=WL-2=17

ODT must be held HIGH for at least ODTH4 after assertion (T1). ODTH is measured from ODT first registered HIGH to ODT first registered LOW, or from registration of Write command. Note that ODTH4 should be adjusted depending on CRC or 2tCK preamble setting

3.2.3 ODT during Reads:

As the DDR4 SDRAM can not terminate and drive at the same time. RTT may nominally not be enabled until the end of the postamble as shown in the example below. As shown in Figure 174 below at cycle T25, DRAM turns on the termination when it stops driving which is determined by tHZ. If DRAM stops driving early (i.e tHZ is early) then tADC,min timing may apply. If DRAM stops driving late (i.e tHZ is late) then DRAM complies with tADC,max timing.

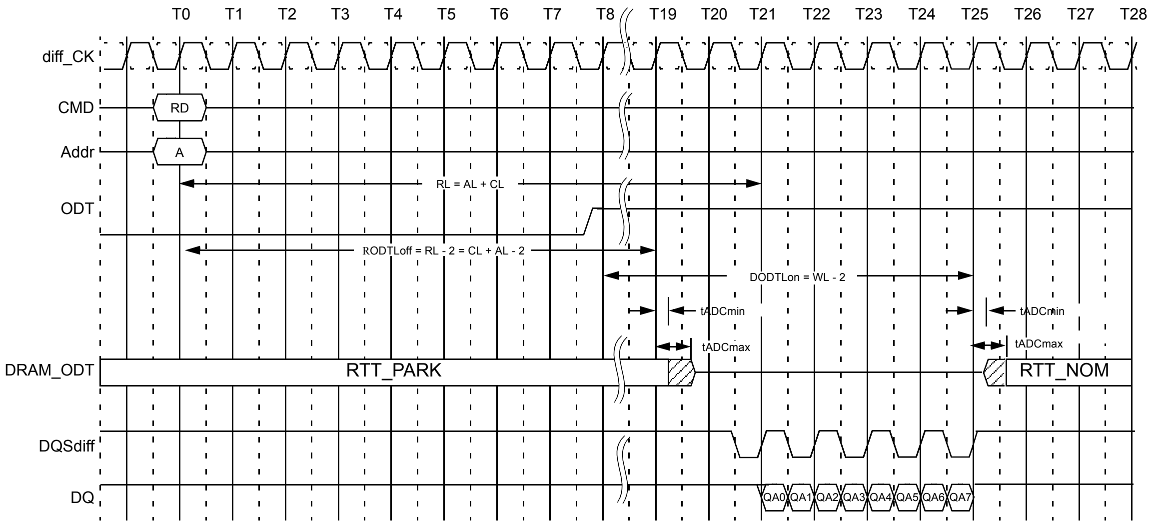


Figure 175. Example: CL=11, PL=0; AL=CL-1=10; RL=AL+PL+CL=21; CWL=9; DODTLon=AL+CWL-2=17; DODTLoff=AL+CWL-2=17;1tCK preamble)

3.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR4 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

3.3.1 Functional Description

The Dynamic ODT Mode is enabled if bit A[9] or A[10] of MR2 is set to '1'. The function is described as follows:
• Three RTT values are available: RTT_NOM, RTT_PARK and RTT_WR.
 - The value for RTT_NOM is preselected via bits A[10:8] in MR1
 - The value for RTT_PARK is preselected via bits A[8:6] in MR5
 - The value for RTT_WR is preselected via bits A[10:9] in MR2
• During operation without commands, the termination is controlled as follows;
 - Nominal termination strength RTT_NOM or RTT_PARK is selected.
 - RTT_NOM on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff and RTT_PARK is on when ODT is LOW.
• When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
 - A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
 - A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_WR is de-selected.
 - 1 or 2 clocks will be added or subtracted into/from ODTLcwn8 and ODTLcwn4 depending on CRC and/or 2tCK preamble setting.
Table 79 shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The Dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10,A9}={0,0} externally.

[Table 94] Latencies and timing parameters relevant for Dynamic ODT with 1tCK preamble mode and CRC disabled

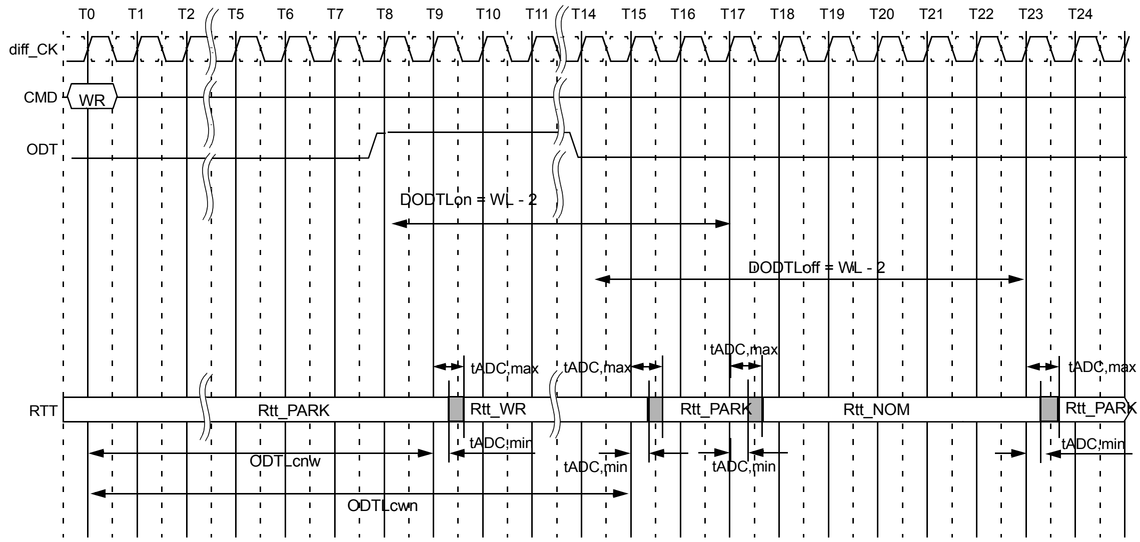
Name and Description	Abbr.	Defined from	Define to	Definition for all DDR4 speed bins	Unit
ODT Latency for changing from RTT_PARK/RTT_NOM to RTT_WR	ODTLcnw	Registering external write command	Change RTT strength from RTT_PARK/ RTT_Nom to RTT_WR	ODTLcnw = WL - 2	tCK
ODT Latency for change from RTT_WR to RTT_PARK/ RTT_Nom (BL = 4)	ODTLcwn4	Registering external write command	Change RTT strength from RTT_WR to RTT_PARK/RTT_Nom	ODTLcwn4 = 4 + ODTLcnw	tCK
ODT Latency for change from RTT_WR to RTT_PARK/ RTT_Nom (BL = 8)	ODTLcwn8	registering external write command	Change RTT strength from RTT_WR to RTT_PARK/RTT_Nom	ODTLcwn8 = 6 + ODTLcnw	tCK(avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	tADC(min) = 0.3 tADC(max) = 0.7	tCK(avg)

[Table 95] Latencies and timing parameters relevant for Dynamic ODT with 1 and 2tCK preamble mode and CRC en/disabled

Symbol	1tck Preamble		2tck Preamble		Unit
	CRC off	CRC on	CRC off	CRC on	
ODTLcnw	WL - 2	WL - 2	WL - 3	WL - 3	tCK
ODTLcwn4	ODTLcnw +4	ODTLcnw +7	ODTLcnw +5	ODTLcnw +8	
ODTLcwn8	ODTLcnw +6	ODTLcnw +7	ODTLcnw +7	ODTLcnw +8	

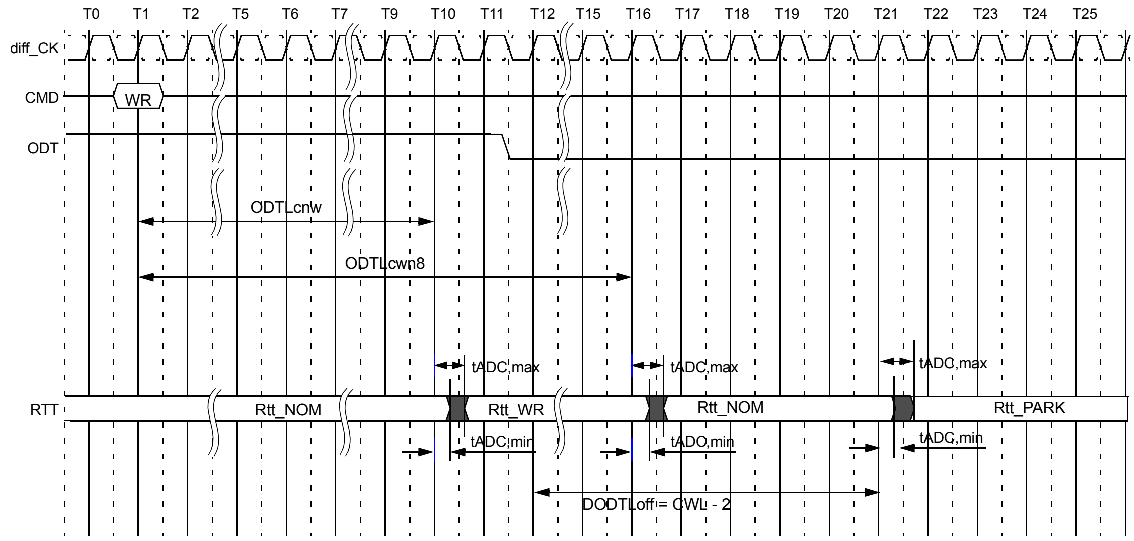
3.3.2 ODT Timing Diagrams

The following pages provide example timing diagrams



ODTLcnw = WL-2 (1tCK preamble), WL-3 (2tCK preamble)
ODTLcwn = WL+2 (BC4), WL+4(BL8) w/o CRC or WL+5,5 (BC4, BL8 respectively) when CRC is enabled.

Figure 176. ODT timing (Dynamic ODT, 1tCK preamble, CL=14, CWL=11, BL=8, AL=0, CRC Disabled)



Behavior with WR command is issued while ODT being registered high.

Figure 177. Dynamic ODT overlapped with Rtt_NOM (CL=14, CWL=11, BL=8, AL=0, CRC Disabled)

3.4 Asynchronous ODT mode

Asynchronous ODT mode is selected when DLL is disabled by MR1 bit A0='0'b.
In asynchronous ODT timing mode, internal ODT command is not delayed by either the Additive latency (AL) or relative to the external ODT signal (RTT_NOM).
In asynchronous ODT mode, the following timing parameters apply tAONAS,min, max, tAOFAS,min,max.

Minimum RTT_NOM turn-on time (tAONASmin) is the point in time when the device termination circuit leaves RTT_PARK and ODT resistance begins to change. Maximum RTT_NOM turn on time(tAONASmax) is the point in time when the ODT resistance is reached RTT_NOM.

tAONASmin and tAONASmax are measured from ODT being sampled high.
Minimum RTT_NOM turn-off time (tAOFASmin) is the point in time when the devices termination circuit starts to leave RTT_NOM. Maximum RTT_NOM turn-off time (tAOFASmax) is the point in time when the on-die termination has reached RTT_PARK. tAOFASmin and tAOFASmax are measured from ODT being sampled low.

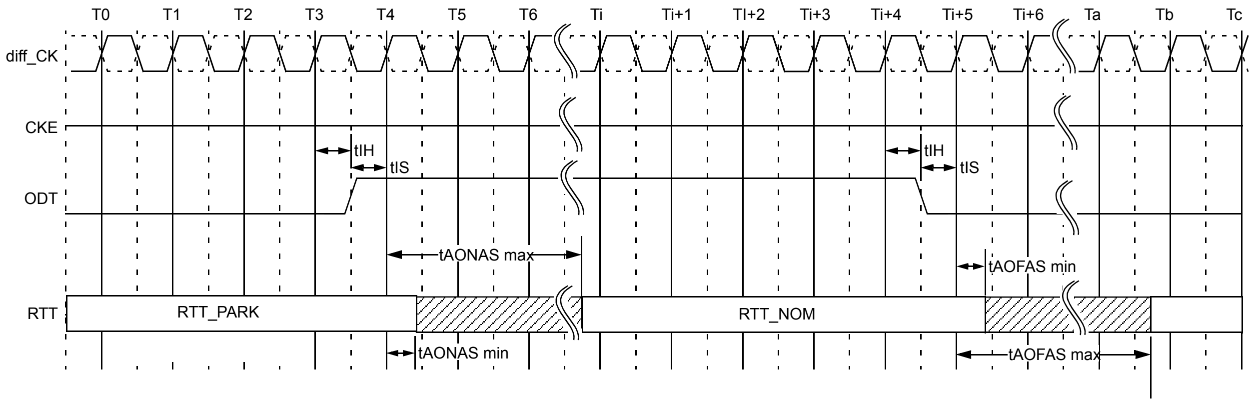


Figure 178. Asynchronous ODT Timing on DDR4 SDRAM with DLL-off

[Table 96] Asynchronous ODT Timing Parameters for all Speed Bins

Description	Symbol	min	max	Unit
Asynchronous RTT turn-on delay	t_{AONAS}	1.0	9.0	ns
Asynchronous RTT turn-off delay	t_{AOFAS}	1.0	9.0	ns

3.5 ODT buffer disabled mode for Power down

DRAM does not provide Rtt_NOM termination during power down when ODT input buffer deactivation mode is enabled in MR5 bit A5. To account for DRAM internal delay on CKE line to disable the ODT buffer and block the sampled output, the host controller must continuously drive ODT to either low or high when entering power down. The ODT signal may be floating after tCPDEDmin has expired. In this mode, RTT_NOM termination corresponding to sampled ODT at the input after CKE is first registered low (and tANPD before that) may not be provided. tANPD is equal to (WL-1) and is counted backwards from PDE.

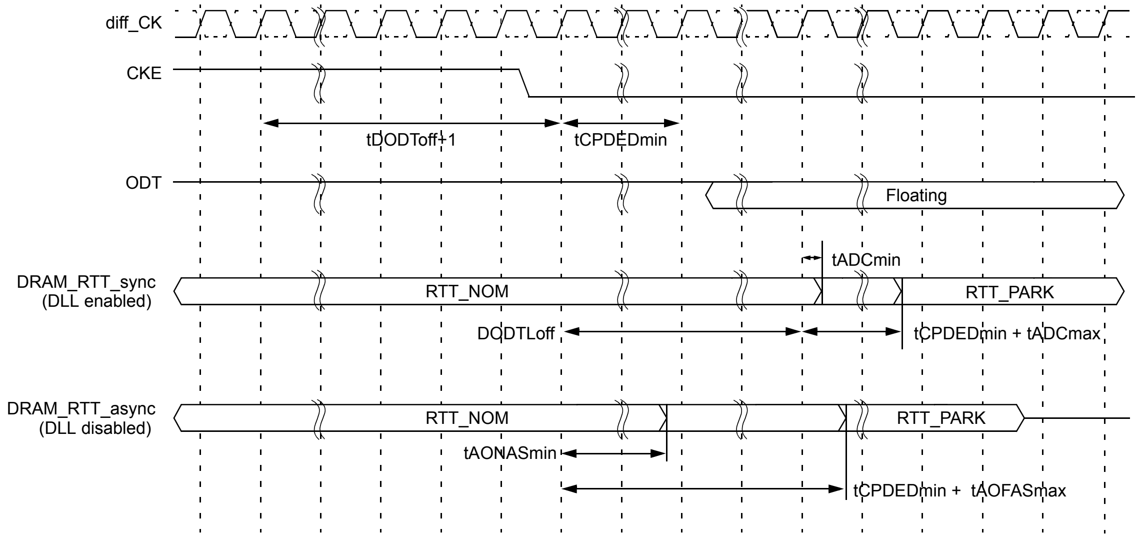


Figure 179. ODT timing for power down entry with ODT buffer disable mode

When exit from power down, along with CKE being registered high, ODT input signal must be re-driven and maintained low until tXP is met.

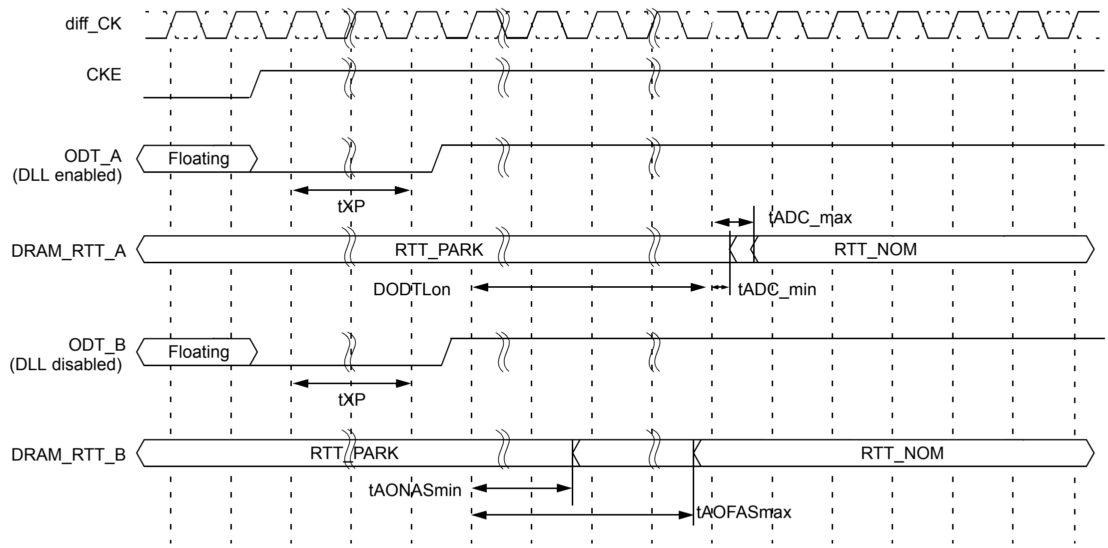


Figure 180. ODT timing for power down exit with ODT buffer disable mode

3.6 ODT Timing Definitions

3.6.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 180.

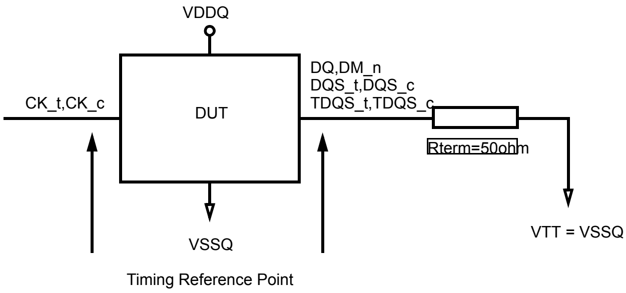


Figure 181. ODT Timing Reference Load

3.6.2 ODT Timing Definitions

Definitions for tADC, tAONAS and tAOFAS are provided in Table 81 and subsequent figures. Measurement reference settings are provided in Table 82. tADC of Dynamic ODT case and Read Disable ODT case are represented by tADC of Direct ODTControl case.

[Table 97] ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure	Note
tADC	Rising edge of CK_t,CK_c defined by the end point of DODTLoff	Extrapolated point at VRTT_NOM	Figure 180	
	Rising edge of CK_t,CK_c defined by the end point of DODTLon	Extrapolated point at VSSQ		
	Rising edge of CK_t - CK_c defined by the end point of ODTLcnw	Extrapolated point at VRTT_NOM	Figure 181	
	Rising edge of CK_t - CK_c defined by the end point of ODTLcwn4 or ODTLcwn8	Extrapolated point at VSSQ		
tAONAS	Rising edge of CK_t,CK_c with ODT being first registered high	Extrapolated point at VSSQ	Figure 182	
tAOFAS	Rising edge of CK_t,CK_c with ODT being first registered low	Extrapolated point at VRTT_NOM		

[Table 98] Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_PARK	RTT_NOM	RTT_WR	Vsw1	Vsw2	Figure	Note
tADC	Disable	RZQ/7	-	0.20V	0.40V	Figure 182	1,2
	-	RZQ/7	Hi-Z	0.20V	0.40V	Figure 183	1,3
tAONAS	Disable	RZQ/7	-	0.20V	0.40V	Figure 184	1,2
tAOFAS	Disable	RZQ/7	-	0.20V	0.40V		

NOTE :

1 MR setting is as follows.
- MR1 A10=1, A9=1, A8=1 (RTT_NOM_Setting)
- MR5 A8=0 , A7=0, A6=0 (RTT_PARK Setting)
- MR2 A11=0, A10=1, A9=1 (RTT_WR Setting)

2 ODT state change is controlled by ODT pin.

3 ODT state change is controlled by Write Command.

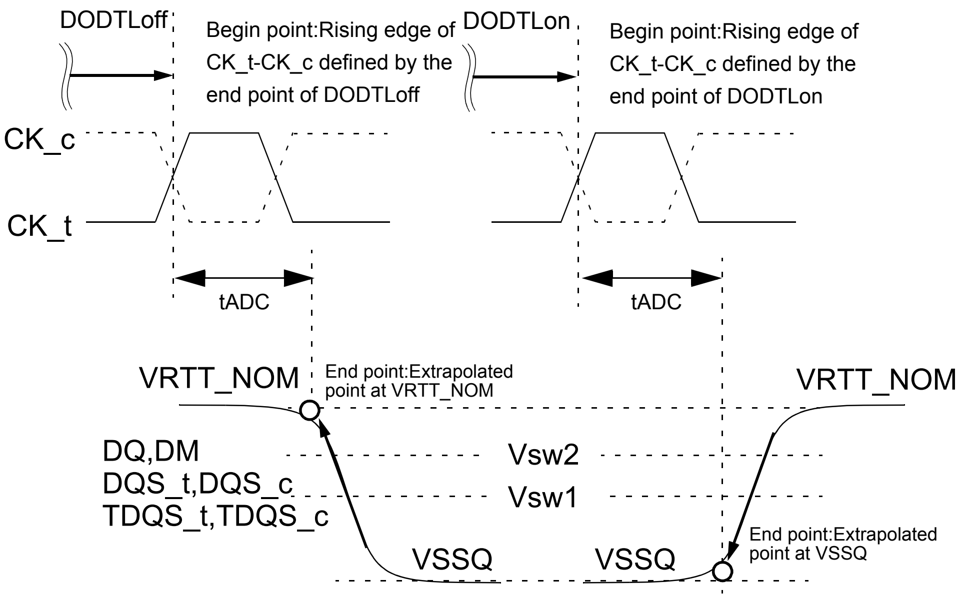


Figure 182. Definition of tADC at Direct ODT Control

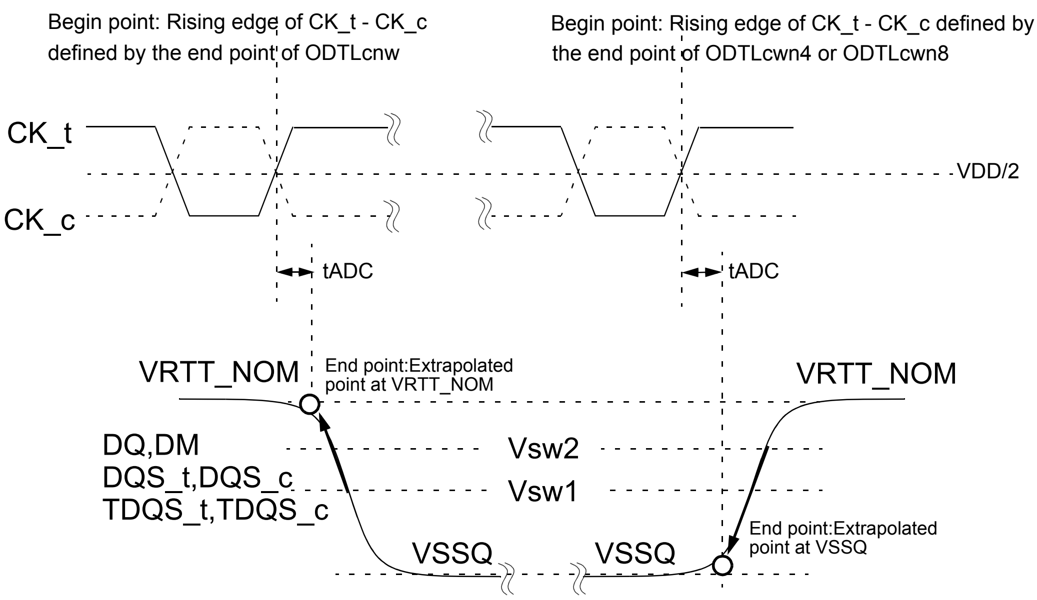


Figure 183. Definition of tADC at Dynamic ODT Control

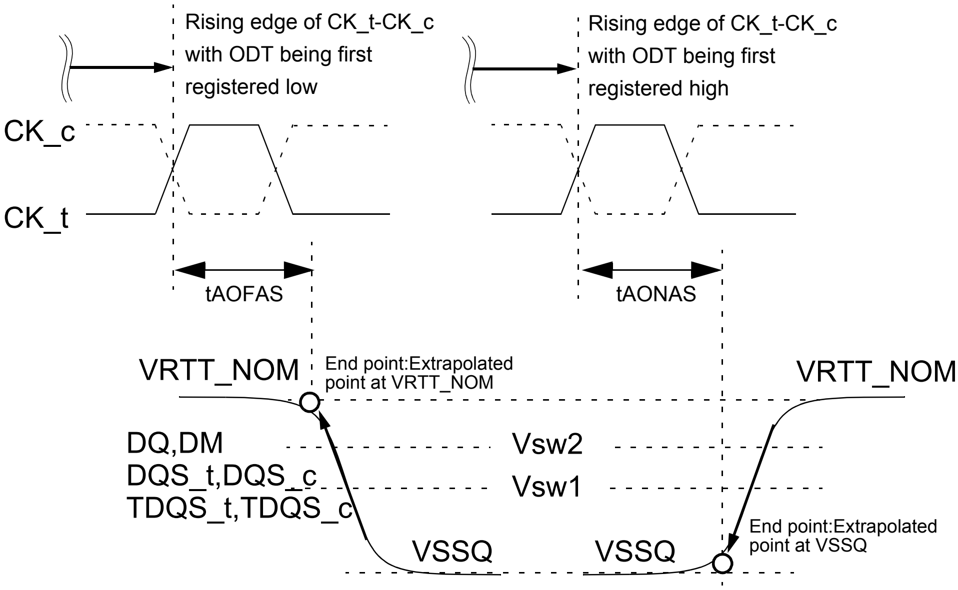


Figure 184. Definition of tAOFAS and tAONAS